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A Simulation of The Applied Bias Effect of Tunnelling Probability in Quadruple Barrier Si/SiO_2 System

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Abstract--- **Recently, multiple quantum wells structure are often used in the laser and diode applications in order to increase their efficiency. In this structure, electron tunnelling phenomena from a quantum well to another well play a key role in electronic transport itself. Tunnelling is a quantum mechanical phenomenon where an electron is commonly represented by its wavefunction. This paper presents a numerical simulation of electron tunnelling probability on three quantum wells (quadruple barrier) Si/SiO_2 system focusing the applied bias effect on the tunnelling probability. The tunneling probability is calculated by solving the Schrodinger's equations through potential barrier using transfer matrix method. The simulation results show the mini-band formation due to the appearance of discrete energy group. We also found that the applied bias on this structure causes the changes in tunnelling probability and discrete energy gap. Therefore, the control of voltage bias and device structure is required in order to obtain expected characteristic of multiple quantum well structure.**

Keywords----**Tunnelling probability, quadruple barrier Si/SiO_2, mini-band formation.**

I. INTRODUCTION

A superlattice is one of an interesting device structure, which has been used in the laser diode and photodetectors application. The superlattice structure is formed when thin multi barriers and multi quantum wells structure are sandwitch periodically [1]. Recent modern fabrication technology allows us for the fabrication of superlattice structure from various material such as GaAs/AlGaAs or Si/SiO_2. The tunnelling phenomenon is very important in this structure, especially how the electron tunnels through the potential barriers and its probability.

In the discussion on tunnelling probability, the effect of applied bias is important to be understood. So far, the investigation of tunnelling probability in resonant tunneling devices (RTDs) consisting of single and double wells have been reported both in experimental and simulation [2]-[6]. In this work, we investigate the tunnelling probability on the three quantum wells (quadratuple barriers) Si/SiO_2 structure, especially the applied bias effect on the probability. The calculation is done based on the solution of Schrodinger equation. In order to understand deeply this structure, this paper also presents the influence of the barriers and potential well thickness on tunnelling probability.

II. SIMULATION METHOD

The structure which forms quadruple tunnel potential Si/SiO_2 is schematically shown in Fig. 1(a). The structure consists of two heavily doped n^+ Si layers in the edges (right and left), four SiO_2 layers and the three low-doped Si layers regions. The conduction band energy for this structure is shown in Fig. 1(b). Consider the electron affinity of Si is 4.05 eV, and that of SiO_2 is 0.9 eV, it is obtained that potential barrier height is 3.15 eV. As a result, the three quantum wells are formed in the silicon layers. Here, the width of Si and SiO_2 layers is designed to be 10 nm and 5 nm, respectively.

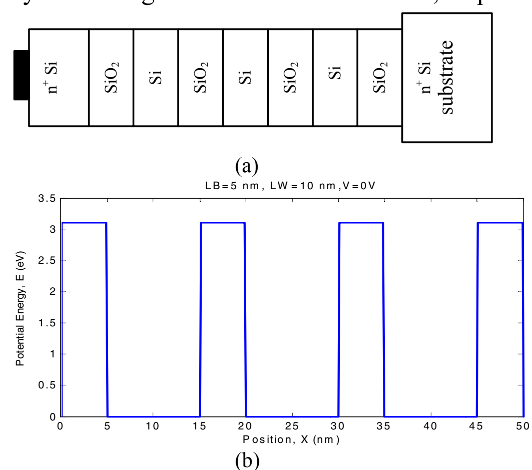

Fig.1 (a) The structure of quadruple Si/SiO_2 barriers and (b) The conduction band energy diagram

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To calculate an electron tunnelling probability, we apply Schrodinger equation in quadruple Si/SiO_2 barriers. The equation is directly solved based on transfer matrix method [7]-[9]. Such method is usually used to calculate the tunnelling probability in Resonance Tunnelling Diode (RTD) structure. By this method, the resonance tunnelling phenomenon which is induced by the interference of electron wave, can be appeared. The transfer matrix method is mainly explained using Fig.2 as follows.

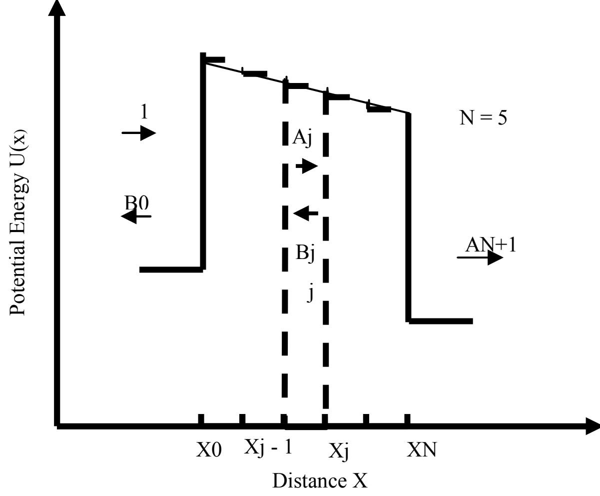

Fig. 2 Energy band diagram of quadruple Si/SiO_2 barriers system

Consider the Fig. 2, electron wave function $_j$ in the point j moving in x direction can be expressed by

$$\psi_j(x) = A_j \exp(ik_j x) + B_j \exp(-ik_j x) \tag{1}$$

where

$$k_j = \sqrt{\left[2m_j^*(E - U_j)/\hbar\right]}$$

Here m^*_j is the effective mass, U_j is the potential energy barrier, E is the electron energy, , and ħ is the reduce Planck's constant.

Consider the continuity of $_j$ and $(1/m^*_j)$ (d $_j$/dx) at each boundary of Si/SiO_2, Aj and Bj in eq.(1) can be calculated from the following equation

$$\begin{pmatrix} A_j \\ B_j \end{pmatrix} = \prod_{i=0}^{j-1} M_i \begin{pmatrix} A_0 \\ B_0 \end{pmatrix} \tag{2}$$

where

$$M_i = \frac{1}{2}\begin{bmatrix} (1+S_i)\exp[-i(k_{i+1}-k_i)x_i] & (1-S_i)\exp[-i(k_{i+1}+k_i)x_i] \\ (1-S_i)\exp[i(k_{i-1}+k_i)x_i] & (1+S_i)\exp[i(k_{i-1}-k_1)x_i] \end{bmatrix} \tag{3}$$

and

$$S_i = \frac{m_{i+1}^*}{m_i^*}\frac{k_i}{k_{i+1}}$$

It can be seen in eq. (3) that M_i is 2 × 2 matrices and N+1 of M matrix is needed in order to obtain the values of A and B in the position of point N (see Fig. 2). Here, N is the total number of grid. By assuming that the amplitude A_0=1 and B_{N+1}=0 (no reflection in point N+1) in Eq. (2) for j=N+1, the tunnelling amplitude A_{N+1} and the tunnelling probability T(E) can be calculated as follows:

$$A_{N+1} = \frac{m_{N+1}^*}{m_0^*}\frac{k_0}{k_{N+1}}\frac{1}{M_{22}} \tag{4}$$

$$T(E) = \frac{m_0^*}{m_{N+1}^*}\frac{k_{N+1}}{k_0}\left|A_{N+1}\right|^2 \tag{5}$$

where $M = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} = \prod_{i=0}^{N} M_i$

III. RESULTS AND DISCUSSIONS

The simulation program has been executed on the various applied voltage (Vapp), barrier thickness (LB), and quantum well thickness (Lw). Here, we use the Si and SiO_2 effective masses of 0.26 and 0.7, respectively. The tunnelling probability is investigated for the range of discrete energy from 0 to 2.48 eV. This limited energy is applied because the presence of unusual phenomenon, which will be explained in the next paper. Fig. 3 shows the energy band diagram (a) and calculated tunnelling probability (b) obtained from the device with barrier width of 4 nm, well width of 10 nm, and applied voltage of 0.2 V.

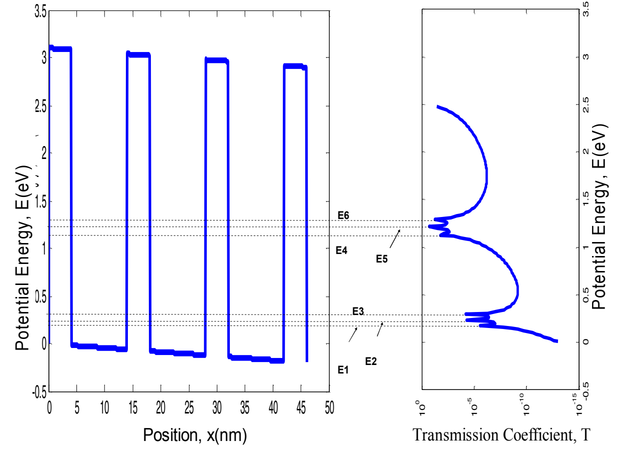

Fig.3 The mini-band formation on 4-barrier Si/SiO_2 structure with Vapp = 0.2V, LB = 4 nm, and LW = 10 nm.

In Fig. 3, it can be seen that the tunnelling probability has two big peaks, i.e. peak at around 0.2 eV and one at around 1.3 eV. Each peak has three small peaks, i.e., peaks E1, E2 and E3 on lower big peaks and peaks E4, E5 and E6 on the bigger one. Therefore, each small peak (E1-E6) is attributed to generated-energy level, as shown in Fig. 3(a). The lower and bigger groups of energy levels like mini-band as well as one formed superlattice structure. The tunnelling probability value of each peak (E1-E6) is called as T1-T6, respectively.

Fig. 4 shows the tunnelling probability vs energy graph obtained from applied bias, Vapp = 0.1 V (a) and Vapp = 0.4 V (b). The other parameter is potential barrier width (LB) = 5

nm, and quantum well width (LW) = 10 nm. For Vapp = 0 V (Fig.4 (a)), there are two big peaks (mini-bands) and each of peak splits to three small peak. It is also found that, for Vapp = 0.5 V (fig. 4(b)), there are three big peaks that also split to small peak discrete energies.

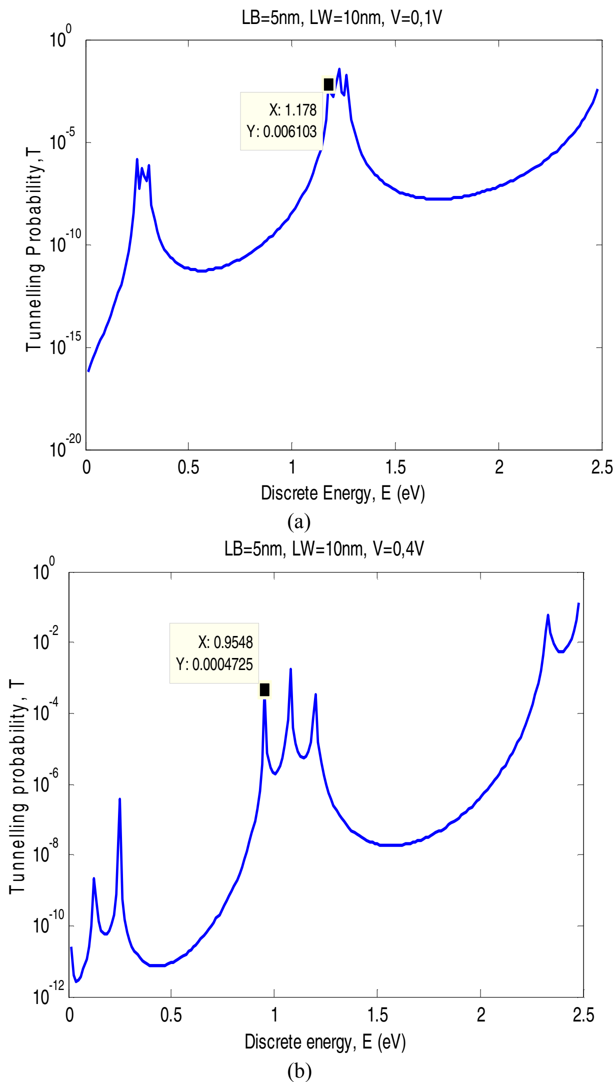

Fig.4 The influence of applied bias on tunnelling probability at (a) Vapp = 0V and (b) Vapp = 1 V.

To compare both graphs, we can analyze the first split energy in the second mini-band. In Fig. 4(a), the indicated point E4 shows the tunnelling probability value of 0.006103 and E of 1.178 eV, whereas in Fig. 4(b), the tunnelling probability of 0.0004725 and E of 0.9548 eV. It means that the increase of applied bias causes the decrease of tunnelling probability and discrete energy.

Fig. 5 shows the change of the tunnelling probability when the applied bias is varied from 0 to 10 V. The general phenomenon in the graph shows the tendency of the decrease in tunnelling probability due the applied bias increase.

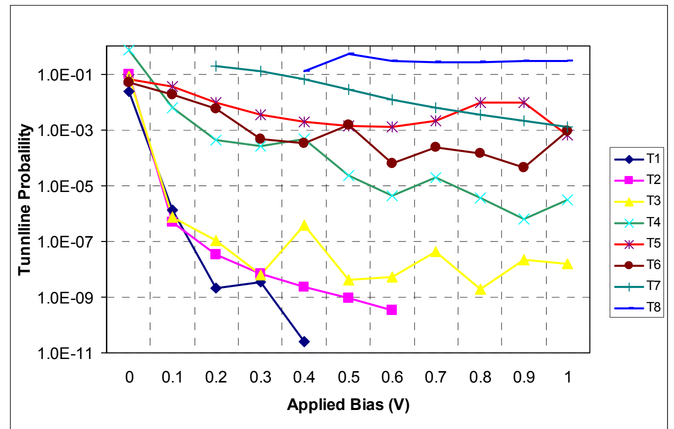

Fig.5 The change of tunneling probability caused the applied bias. The bias is applied from 0 – 1 V with LB = 5 nm and LW = 10 nm.

The influence of barrier thickness on the tunnelling probability is shown in fig. 6, where the parameter LW = 10 nm and Vapp = 0.5 V. It shows the decrease of tunnelling probability level due to the increase the barrier thickness. For example, let's consider the line T2. The tunnelling probability is found to be 0.1 for LB = 1 nm and around 10^{-20} for LB = 10 nm.

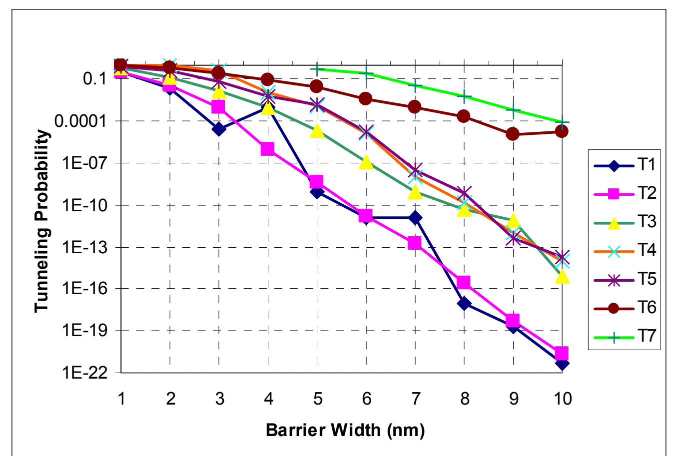

Fig.6 The influence of barrier thickness on tunneling probability with Vapp = 0.5V and LW 10 nm.

The influence of the well width on the tunnelling probability is shown in fig. 7, where parameter LB = 10 nm and Vapp = 0.5 V. this result is almost the same phenomena with that in Fig. 6, i.e., is the increase of quantum well width causes the decrease of tunnelling probability.

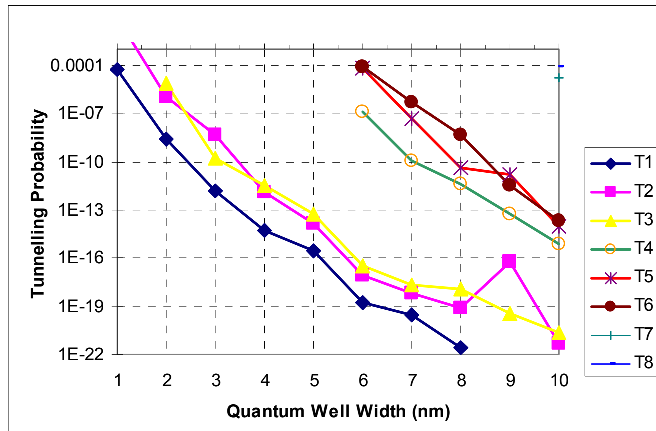

Fig. 7 The influence of the quantum well width to tunneling probability with Vapp = 0.5V and LB is 10 nm.

IV. CONCLUSIONS

We have studied the effect of applied bias, the barrier thickness, and the quantum well width on the tunnelling probability in quadruple barriers Si/SiO_2 system. The calculation was done based on transfer matrix method. The simulation results show that the increase of applied bias, barrier thickness and quantum well width causes the decrease of tunnelling probability. The results also show the mini-band formation due to the appearance of discrete energy group. Therefore, the control of voltage bias, barrier thickness and quantum well width is required in order to obtain the expected performance of the quadruple Si/SiO_2 system.

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