Observation of Negative Differential Conductance in Nanoscale *p-n* Junctions

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***Abstract*---Recently, *p-n* junction characteristics in nanometer scale have been investigated in relation with photonics and electronics applications. In this paper, we report the experimental observation of negative differential conductance (NDC), the basic indication of tunneling, in nanoscale *p-n* junctions under forward bias condition. The NDC has been observed only at low temperatures, suggesting that tunneling is mediated by some states in the band gap, most likely by individual dopants with deeper energy levels compared to bulk. Furthermore, we also observed random telegraph signal (RTS) at low temperatures, which is ascribed to sudden changes of charge states of an individual dopant. These results illustrate the nature of individual dopants in nanoscale *p-n* junctions and their impact on device characteristics.**

Keywords---*NDC; tunneling; nanoscale p-n junction; individual dopant.*

I. INTRODUCTION

Reduction in Si MOSFET dimensions brings several difficulties in conventional device operation [1]. By decreasing device size, operating voltage will be lowered, but it is difficult to appropriately maintain a good on/off current ratio. In order to overcome this problem, it is proposed that the transport mechanism must be drastically changed from the conventional thermionic-emission transport and that tunnel field-effect transistors (TFETs) are promising candidates for improving the operation conditions.

Tunneling is a quantum mechanical effect, where electrons (holes) have a finite probability of transmission through an energy barrier and this effect becomes most pronounced in nanometer-scale structures. In *p-n* junctions, tunneling mechanism can be observed both under reverse and forward bias. Tunneling mechanism under reverse-bias mode, so-called Zener tunneling, is inter-band tunneling, as indicated by a rapid increase of current. It is basically the main tunneling mechanism in TFETs [2-4].

Under forward bias for heavily doped (degenerated) *p-n* junctions, there is another inter band tunneling mechanism, which is the basis of Esaki tunneling diodes [5]. The tunneling in forward-bias mode can be seen as negative differential conductance (NDC), i.e, a negative slope in current-voltage (*I-V*) curve. So far, tunneling in nanometer-scale *p-n* junctions has been reported in vertical nanowires in forward-bias mode [6,7] and in lateral gated *p-n* junctions in reverse-bias mode [8]. In this work, we study nanoscale lateral *p-n* junctions in forward-bias mode and report the experimental observation of NDC at low temperatures. RTS has also been observed at low temperatures, indicating the effect of a single charge trap. We ascribe these phenomena to the influence of individual dopants on the electrical characteristics.

II. DEVICE STRUCTURE AND MEASUREMENT SETUP

We fabricated nanoscale silicon-on-insulator (SOI) *p-n* junctions. Figure 1 shows schematically the device structure and *I-V* measurement setup. Nanowires were patterned on the SOI layer by an electron beam (EB) lithography technique. Then, a selective doping technique was used to create the *n*-type (phosphorus-doped) and *p*-type (boron-doped) regions. The channel thickness is about 10 nm, while the device length and width are 1000 nm and 150 nm, respectively. Aluminum contact pads were formed as electrodes.

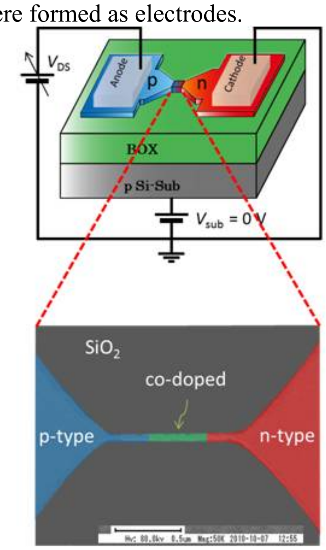

Fig. 1. (a) Device structure and bias configuration for electrical characterization. (b) Co-doped devices, based on SEM images. Co-doped region is located within the thin and narrow nanowire.

The *n*-type region was doped with phosphorus (P) to the concentration $N_D \approx 1.0 \times 10^{18}$ cm^{-3}, while the *p*-type region was doped with boron (B) to the concentration $N_A \approx$

1.5×10^{18} cm^{-3}. A co-doped region, doped with both P and B, is designed in the center of the nanowire. The *p*-Si substrate was weakly *p*-type, doped with boron ($N_A \approx 1.5\times10^{15}$ cm^{-3}). The thickness of the buried oxide layer between the nanowire and the substrate is 150 nm. The nanowire is covered with a 10-nm-thick SiO_2 layer, grown by thermal oxidation. Devices were measured in a vacuum chamber of an electrical measurement system. The *p*-type region is positively biased for these measurements, i.e., the *p-n* junction is forward-biased, while the *n*-type region and substrate are grounded.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

We measured current versus applied bias (*I-V*) characteristics in the dark condition. The measurement results are shown in Fig. 2. *I-V* characteristics at room temperature (T = 300 K), as shown in Fig. 2(a), are similar to the conventional diode behavior, although parasitic resistance due to the narrow wire dimension causes suppression of current and shift the current onset.

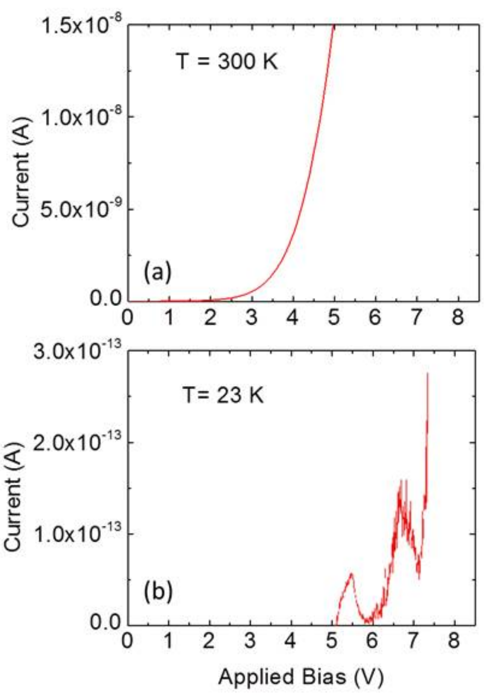

Fig. 2. *I-V* characteristics in forward bias at different temperatures: (a) T = 300 K and (b) T = 23 K. For T = 23 K, NDC can be observed.

At low temperatures, as shown in Fig. 2(b), the voltage for the current onset is further shifted compared to the room temperature behavior. This is caused by the dopant freeze-out effect [9], which leads to an effectively smaller dopant concentration. However, it is even more important to note that, at T = 23 K, *I-V* characteristics exhibit NDC. This behavior, except for the observation of a second peak, is similar to Esaki-diode characteristics, suggesting that the observed features are most likely due to resonant tunneling phenomena in the *p-n* junction. However, since doping concentration of our devices is lower than the doping levels known for Esaki diodes, NDC may occur by a different mechanism. Based on the fact that NDC has been observed just at low temperature, it is likely that tunneling is mediated by some states in the band gap, most likely by individual dopants.

In other devices, a different type of behavior could be also observed. We measured *I-V* characteristic at room temperature and several temperatures below 100 K in the dark condition. Figure 3(a) shows the *I-V* characteristics at T = 300 K and at low temperature (T = 10 K). We observed current fluctuations in *I-V* characteristics at temperatures below 30 K. These current fluctuations can be ascribed to charge trapping and de-trapping by a single trap site. At different temperatures, time dependence of the current was measured as a function of applied bias. The data at 10 K are shown in Fig. 3(b). Random telegraph signals (RTS) with two levels were clearly observed, suggesting that the trap is most likely a single dopant, which can have only two possible states. The RTS frequency is increased by increasing the forward bias, indicating that the RTS (trapping and de-trapping) is sensitive to the change of electric field near the *p-n* junction. Therefore, a single dopant located in the depletion region may be responsible for the RTS.

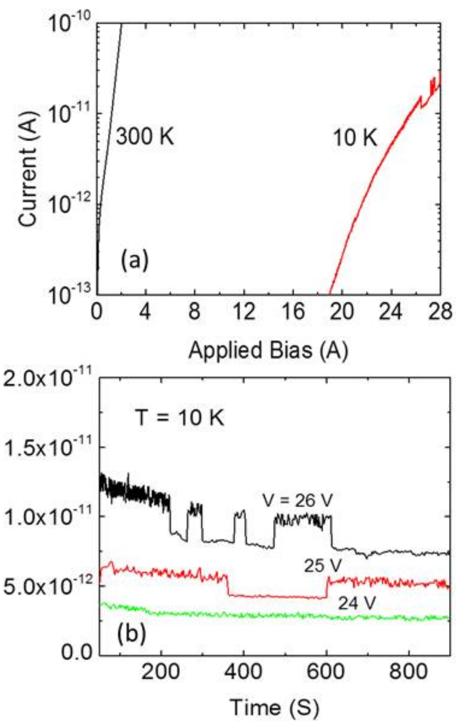

Fig. 3. (a) *I-V* characteristics in forward bias at temperature 300 K and 10 K. For $T = 23$ K, current fluctuations has been observed. (b) Examples of *I*-time characteristics at $T = 10$ K for different applied biases. Two-level RTS can be seen above a certain forward bias.

As mentioned above, we observed NDC and RTS in *I-V* characteristics in the low-temperature measurements. These behaviors may show the nature of individual dopant under forward bias in nanoscale *p-n* junctions. We can analyze the origin of both behaviors from the energy diagram of the devices, as schematically shown in Fig. 4. In thermal equilibrium, the Fermi levels in the *p*-type and *n*-type are aligned. When positive bias is applied to the *p*-type region, as in the forward-bias case, the Fermi level of the *p*-type will be shifted downwards and current starts to flow. Starting from this situation, we can analyze two different cases. The first case is the existence of a pair of deep dopants in the depletion layer, as shown in Fig. 4(a). An electron moving from the *n*-type to the *p*-type region, as part of the diffusion current, may be trapped by an ionized deep donor in the depletion layer. A similar behavior may also occur for a hole, which may be trapped by a deep acceptor. In a certain forward bias, the ground states of the deep donor and the deep acceptor are aligned and, therefore, the electron can resonantly recombine with the hole. By further increasing the forward bias, the resonant recombination condition turns off, resulting in the reduction of the forward current, i.e., NDC. The second peak, which has been observed at different applied bias, may indicate the existence of a second pair of deep dopants. This second pair of dopant, with different energy level, provide different noise feature, as shown in Fig. 2(b). The background current increasing with applied forward bias is an ordinary diffusion current in the *p-n* diode.

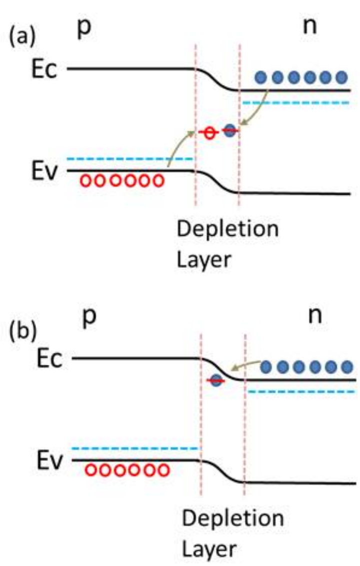

Fig. 4. Band diagrams of *p-n* junction under forward bias. Two different cases are illustrated: (a) when a pair of opposite-type deep dopants mediates transport and (b) when one type of dopant, located in depletion layer, works as a charge trap.

A second case, shown in Fig. 4(b), is when a single dopant in the depletion layer works as a charge trap. In this situation, a pair of a donor and an acceptor is not relevant, but only a single dopant nearby the edge of the depletion layer works as a charge trap. The trapped carrier can escape from the dopant due to thermal activation [9]. These trapping and de-trapping events of a carrier cause potential fluctuations, i.e., RTS. Further investigation is required to fully clarify the origin of this phenomenon.

As illustrated above, the observations of NDC features and discrete-level RTS can be associated with the effects of discrete dopants on the nanoscale *p-n* junction's electrical characteristics. These results provide further evidence about the enhanced importance of the discrete dopants in the transport mechanisms in nanoscale devices, as we reported previously [10-13]. These findings also suggest that there is a rich variety of phenomena emerging when the basic structure of the *p-n* junction is scaled down into nanometer-order dimensions. This is promising for future applications that combine the well-established conventional *p-n* junction theory and technology with novel physics phenomena specific to the nanoscale.

IV. CONCLUSIONS

We report negative differential conductance and random telegraph signals observed in nanoscale *p-n* junctions under forward bias condition. These features are most likely caused by the effects of individual dopants, suggesting the important role that the discreteness of dopant distribution plays in nanoscale. The present results may contribute to the development of dopant-based tunneling FETs on the basis of the nanostructured *p-n* junctions.

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