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Dopant-induced random telegraph signal in nanoscale lateral silicon *pn* diodes at low temperatures

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We studied current-voltage characteristics of nanoscale *pn* diodes having the junction formed in a laterally patterned ultrathin silicon-on-insulator layer. At temperatures below 30 K, we observed random telegraph signal (RTS) in a range of forward bias. Since RTS is observed only for *pn* diodes, but not for *pin* diodes, one dopant among phosphorus donors or boron acceptors facing across the junction is likely responsible for potential changes affecting the current. Based also on potential measurements by low-temperature Kelvin probe force microscope, RTS is ascribed to trapping/detrapping of carriers by/from a single dopant near the farther edge of the depletion region. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4841735]

Nanoscale *pn* diodes have significant advantages over conventional diodes because of their low-dimensional potential profiles and unique structural properties. Recently, a variety of topics related to downsized *pn* diodes have been extensively studied, i.e., interband tunneling in vertical and lateral Si nanodiodes,[1,2] nanoscale avalanche photodiodes,[3] radial *pn* junction nanorods for solar cell applications,[4] and fundamental properties of two-dimensional *pn* junctions.[5,6] However, there is another important aspect in doped nanoscale devices. With miniaturization of Si devices, the number of dopants is also reduced, and one or a few dopants may strongly affect the electrical characteristics of the devices. In fact, it is reported that in metal-oxide-semiconductor field-effect transistors (MOSFETs), single dopant atoms (donor or acceptor) in the channel determine the device characteristics.[7–9] In contrast, effects of discrete dopants have not been reported in *pn* diodes, except for a report on photo-induced fluctuations of diode current.[10]

By further reduction in size of *pn* diodes, however, the discreteness of dopants will undoubtedly gain an even more significant role in the diode characteristics. In this work, our purpose is to identify signatures of individual dopants in the current-voltage (*I-V*) characteristics of nanoscale Si *pn* and *pin* diodes at different temperatures, in the dark condition. As a result, we observe random telegraph signal (RTS) at low temperatures, only for *pn* diodes. Based on this fact and supporting results obtained by Kelvin probe force microscopy (KFM), the RTS is ascribed to trapping/detrapping of a charge carrier by/from a single dopant atom in the depletion region of the *pn* junction.

We fabricated, on a silicon-on-insulator (SOI) wafer, lateral *pn* diodes consisting of a *pn* junction, defined in a narrow and thin Si region, coupled to fan-shaped leads (*p*- and *n*-Si) and square-shaped pads, with Al contact electrodes, as shown in Fig. 1(a). As reference devices, we also fabricated on the same sample *pin* diodes containing a nominally intrinsic (*i*) layer between the *n*- and *p*-pads. Electrical characteristics of the *pn* and *pin* diodes were measured by applying a variable voltage to the *p*-region, with the *n*-region and *p*-Si substrate usually grounded. Figures 1(b) and 1(c) show atomic force microscope (AFM) images of *pn* and *pin* diodes, respectively, including the junctions. For both types of diodes, the Si layer thickness is only ~5 nm, the length of the straight-patterned central region is about 1000 nm, and the width is ~200 nm. The buried oxide layer is 150-nm-thick, and a 10-nm-thick SiO_2 layer was thermally grown for passivation, before defining Al contacts for the *p* and *n* leads.

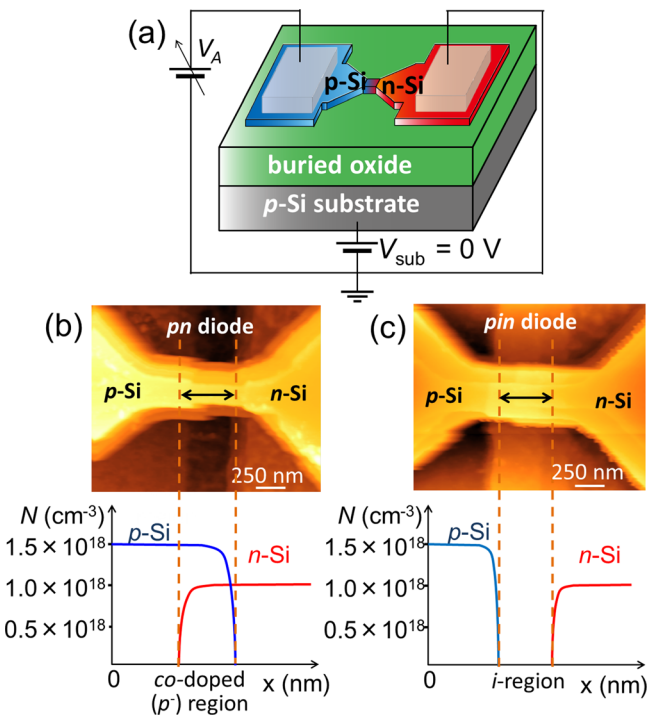

FIG. 1. (a) Device structure of a *pn* diode and measurement setup. (b), (c) AFM images and doping concentration profiles for *pn* junctions (containing a co-doped region) and *pin* junctions (containing an intrinsic region).

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A conventional doping technique, based on thermal diffusion from a spin-coated silicate glass as a dopant source, was used to create phosphorus (P)-doped and boron (B)-doped regions. The lower panels in Figs. 1(b) and 1(c) show expected dopant concentration profiles across the *pn* and *pin* diodes, respectively. P and B concentrations away from the junction are $N_D \approx 1 \times 10^{18}\,cm^{-3}$ and $N_A \approx 1.5 \times 10^{18}\,cm^{-3}$, respectively, as estimated from secondary ion mass spectrometry (SIMS) for thicker (50 nm) reference samples. All of the *pn* diodes contain a co-doped region, doped both with P donors and with B acceptors. Due to the higher concentration of B compared to that of P, the co-doped region is effectively *p*-type, and, therefore, the location of the *pn* junction is at the boundary between the co-doped region and the *n*-Si region. In the *pin* diodes, the *i*-region (nominally undoped) is not ideally intrinsic because the commercial SOI wafers have a native low doping with B ($N_A \approx 1 \times 10^{15}\,cm^{-3}$). However, since the estimated number of B atoms in the *i*-region is one or less, it is reasonable to assume this region as intrinsic.

First, we measured the *I-V* characteristics of *pn* diodes to confirm their general behavior at different temperatures. Figure 2(a) shows that, even in these ultrathin-Si diodes, rectifying behavior is observed in a wide temperature (*T*) range, between 300 and 30 K. With decreasing temperature, it is also seen that the voltage for the onset of forward current increases. This is caused by a reduction of the effective carrier concentration due to dopant freeze-out effect,[11,12] which leads to an increase in the parasitic resistance of the leads. Therefore, at lower temperatures, because a significant amount of the externally applied voltage is consumed in the lead regions, the voltage drop across the *pn* junction is far below the applied voltage. A larger shift of onset-voltages between 150 and 100 K, as seen in Fig. 2(a), is consistent with the fact that the dopant freeze-out effect becomes prominent in this temperature range.[11]

In Fig. 2(b), we compare *I-V* curves measured at low temperatures ($T = 30$ K) for *pn* and *pin* diodes with nominally same designed dimensions. However, due to enhanced oxidation rate of the co-doped region for the *pn* diodes, their cross-sectional area is significantly smaller than for the *pin* diodes. Consequently, current is higher for the *pin* diodes. In the present experiment, 9 *pn* diodes and 9 *pin* diodes were measured in the low-temperature range ($T = 6$–30 K). Discrete current fluctuations can be found only for the *pn* diodes (for 3 different devices), but for none of the *pin* diodes. In the *pin* diodes, electron flux flowing from the *n*-Si region to the *i*-Si region recombines within the *i*-region with the hole flux flowing from the opposite direction. This is the major component of the total current, and the electron flux cannot usually reach the boundary of the *p*-type region without recombination inside the long *i*-region. In such *pin* diode structure, dopants are practically absent in the *i*-region and, therefore, potential barriers for electrons and holes are not expected to fluctuate in time. This different behavior of *pn* and *pin* diodes suggests that dopants, mixed inside the depletion region of a *pn* diode, are most likely the origin of the current fluctuations. This will be further confirmed by KFM, as shown in the latter part of this paper.

Since the effect of individual dopants is expected to become more prominent at low temperatures, we studied the *I-V* curves mainly for $T < 100$ K, as shown in Fig. 3(a). It is found that noise becomes visible in the *I-V* characteristics in a limited bias range, indeed only for low temperatures, below 30 K (as shown in the inset). In Figs. 3(b)–3(d), *I*-time traces are shown for different temperatures, 30, 10, and 6 K, respectively. Applied bias was used as a parameter. For larger applied biases, a drift of the current in time is ascribed to the slow inversion of the *p*-Si layer, due to the low rate of minority carrier generation at these low temperatures. It can be seen that, depending on bias, different behaviors can be found for the current noise. For low biases, the current can be treated as noise-free because the fluctuations have small amplitude (comparable with the noise level, ~10 fA). In a certain bias range, RTS with two discrete current levels is clearly observed. RTS is, in general, associated with charge-state fluctuation of an oxide trap, as reported in a number of important papers on RTS in MOSFETs.[13–16] In these studies, it is usual to extract the properties of the trap from the gate voltage dependence of the RTS. However, in *pn* diodes, a gate is not available. An analysis of the RTS as a function of temperature and bias applied across the *pn* junction is shown next.

Time constants for low (τ_L) and high (τ_H) current levels, extracted from the *I*-time data, are shown in Fig. 3(e) as a function of applied forward bias. It can be seen that both τ_L and τ_H depend on applied bias, despite the larger scattering for the τ_H data. According to the fundamental theory of the Shockley-Read-Hall (SRH) statistics,[17] applied to noise in *pn* junctions,[18] such dependencies indicate that the RTS is due to a generation-recombination center. At the low temperatures of our measurements, due to the strong freeze-out effect, such a center responsible for RTS is likely a dopant located in the depletion region. In fact, the values of the time

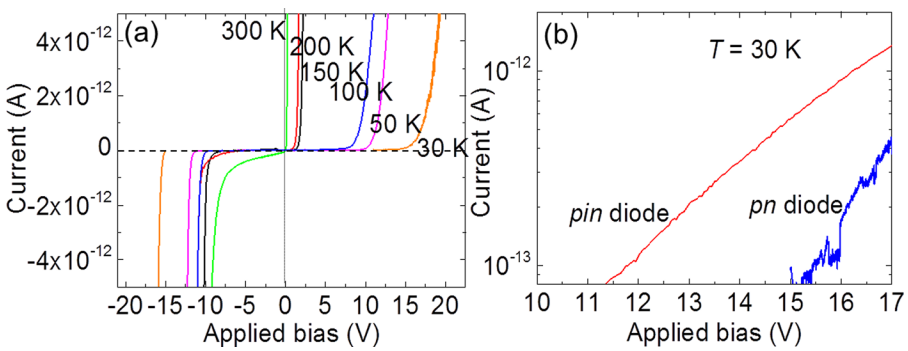

FIG. 2. (a) Temperature dependence of *I-V* characteristics for a *pn* diode under reverse and forward bias. (b) *I-V* characteristics of a *pn* diode and a *pin* diode at low temperature ($T = 30$ K) under forward bias.

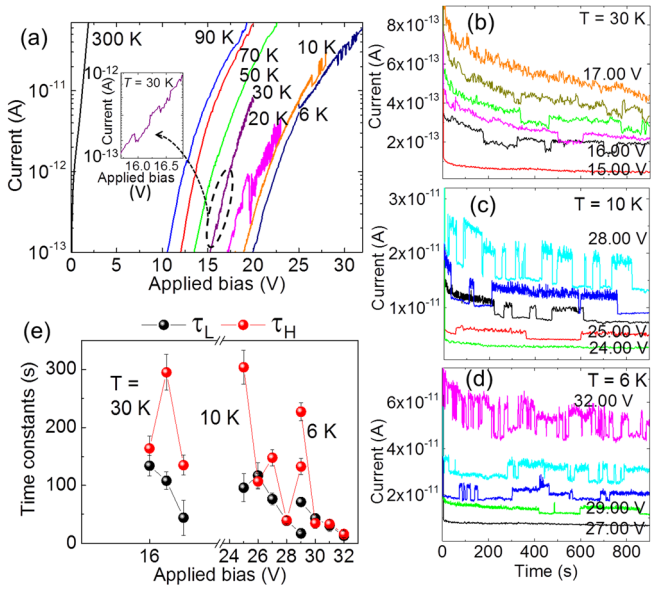

FIG. 3. (a) *I-V* characteristics for a *pn* diode in forward bias at $T < 100\,\mathrm{K}$ (data for 300 K is shown as reference). At low temperatures, *I-V* measurements were stopped at biases not far beyond the bias for noise observation. Inset shows RTS-like features in the data for $T = 30\,\mathrm{K}$. (b), (d) *I*-time traces as a function of applied bias for 30 K (0.25 V step), 10 K (1.0 V step), and, respectively, 6 K (1.0 V step). (e) Time constants, extracted from the *I*-time data for low (τ_L) and high (τ_H) current levels, as a function of applied bias.

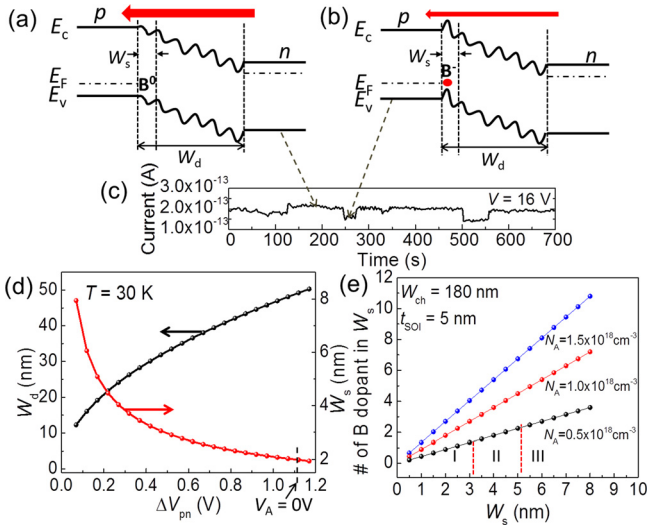

FIG. 4. (a) and (b) Band diagrams of *pn* diodes under forward bias. The band diagrams are drawn based on bulk *pn* junction theory, combined with individual dopant potentials in the depletion region. One B acceptor in different charge states, neutral (B^0) and, respectively, ionized (B^-), affects the electron current flow. (c) Example of RTS in an *I*-time trace. (d) Calculation of depletion region width (W_d) as a function of potential difference between the *p*- and *n*-pads (ΔV_{pn}), based on bulk *pn* junction theory, for $T = 30\,\mathrm{K}$. The width of the "sensitive region" (W_s), as defined in the text, is also plotted. (e) Number of B dopants inside the sensitive region for different values of N_A. Different regimes are outlined depending on the number of B dopants, in particular, for lowest N_A.

constants are consistent with the carrier dwell time in typical shallow dopant atoms, such as P or B, in Si (longer than 10 s at $T < 30\,\mathrm{K}$).[12] The lack of observation of the noise for $T > 30\,\mathrm{K}$ may be due to the fact that the dwell time in dopants becomes shorter than the time resolution of our measurements and the charge state switching cannot be detected. For higher biases, the current starts to fluctuate between three or more levels, with a significantly more complex behavior, suggesting that not only one, but several charge traps are involved.

As indicated above, RTS is likely due to trapping/detrapping of a charge carrier (electron or hole) by/from a single dopant atom. Figures 4(a) and 4(b) illustrate the band diagrams for a forward-bias *pn* diode. For nanoscale *pn* diodes, we combined the theory for bulk *pn* junctions with individual dopant potentials in the depletion region, as schematically illustrated in the diagrams. For simplicity, we consider only electron diffusion current under forward bias condition (It is noted that a symmetrical argument holds for hole current). Although there are a number of dopants in the entire depletion region, the most critical dopant that affects the electron current is only one B atom located near the farther edge (on the *p*-Si side) of the depletion region. This edge of the depletion region is defined as a "sensitive region," as explained in more details later, because the potential here works as a barrier for electrons and limits electron flux entering into the *p*-Si region. While the B dopant remains neutral, B^0 (with a hole captured), a high electron current can flow [Fig. 4(a)]. However, when the B dopant is ionized, B^- (by capturing an electron), the local electronic potential is raised, and the electron current is suppressed to the lower level [Fig. 4(b)].

Next, we evaluate the number of dopants located in this "sensitive region," critically affecting the current. First, the depletion region width (W_d) is calculated based on conventional *pn* junction theory, for $T = 30\,\mathrm{K}$.[11] This is plotted in Fig. 4(d) as a function of the potential difference between the *p* and *n* regions (ΔV_{pn}). In the absence of applied bias ($V_A = 0\,\mathrm{V}$), as marked on the right, W_d is approximately 50 nm. Then, we quantitatively define a "sensitive region" considering the effect of individual dopants inside the depletion region. The sensitive region extends from the left boundary of the depletion region to the right, covering a potential difference of 45 meV. This value basically corresponds to the charging energy of a B acceptor in Si.[19] The width of this sensitive region (W_s) is also plotted in Fig. 4(d). This allows us to evaluate the number of B dopants present inside W_s, as shown in Fig. 4(e). The dopant concentration at the depletion region's boundary is assumed to lie in the range of 0.5×10^{18}–$1.5 \times 10^{18}\,\mathrm{cm}^{-3}$ since the exact value of dopant concentration cannot be directly measured for such an ultrathin Si film. The lowest B concentration ($0.5 \times 10^{18}\,\mathrm{cm}^{-3}$) is, basically, consistent with our experimental data. As indicated on the graph, depending on the number of B dopants found in W_s, three distinct regimes can be identified for this lowest concentration of B. In regime I, no B dopants are included in W_s; accordingly, RTS is not expected. In regime II, the number of B dopants in W_s is around one. This corresponds to the bias range for the observation of the two-level RTS. For regime III, two or more B dopants are incorporated in W_s, resulting in a multiple-level RTS. Thus, this evaluation of the number of critical dopants confirms that the RTS characteristics can be reasonably ascribed to B dopants located nearby the boundary of the depletion region.

For directly observing the potential landscape in nanoscale *pn* junctions, we carried out KFM measurements, as

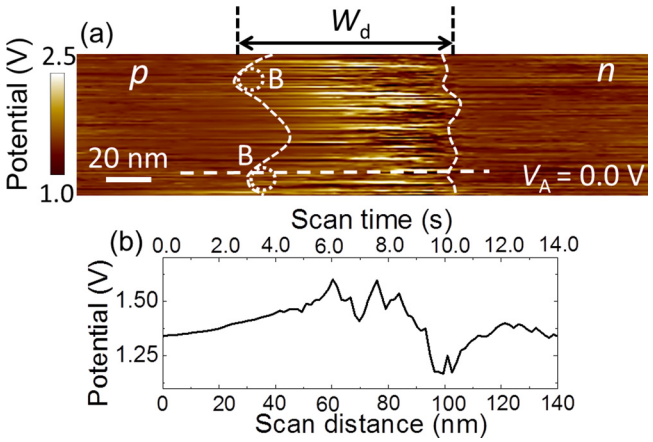

FIG. 5. (a) Electronic potential landscape measured by low-temperature ($T = 15$ K) KFM across a *pn* junction's depletion region. The depletion region is delineated by white dashed boundaries. B dopants are schematically shown at the boundary. (b) Line profile illustrating potential fluctuations as a function of both scan distance and scan time.

described in more details in Ref. 20. Here, in Fig. 5(a), we show a result measured at low temperature ($T = 15$ K) for a *pn* diode, at zero applied bias. A region containing prominent potential fluctuations can be observed between flat-potential areas. We previously demonstrated, based on the applied bias dependence,[20] that this region corresponds to the depletion region of the *pn* diode. Figure 5(b) shows a line profile across the depletion region, in order to illustrate the potential fluctuations localized to the depletion region. Since KFM is a scanning-probe technique, the measurement can be characterized not only as a function of distance but also as a function of time. In Fig. 5(b), scan distance was converted into scan time by knowing the measurement time per point. In this line profile, time-dependent potential fluctuations can be seen as random fluctuations between several levels. Such time-dependent fluctuations can be ascribed to the fluctuations of the charge states of dopants under the electric field formed in the depletion region. Since a number of dopants contribute to this potential, the fluctuations do not occur only between two distinct levels. However, undulations on a scale of $\sim$10 nm are observed at the boundary of the depletion region. These features are consistent with individual dopant potentials (some B acceptors are illustrated in Fig. 5(a)), strongly affecting the boundary of the depletion region.

The KFM results presented here suggest the significant impact of individual dopants in the depletion region, in particular at its boundaries, on the potential landscape of nanoscale *pn* diodes. These findings are basically consistent with our model of a dopant in the depletion region being responsible for the observation of RTS in the *I-V* characteristics.

In conclusion, we fabricated nanoscale ultrathin lateral *pn* junctions and studied their behavior by electrical characterization and potential measurements. We observed currents fluctuations as RTS under forward bias at low temperatures. The RTS is due to potential fluctuations caused by trapping and detrapping of charge carriers by/from individual dopants in the depletion region. KFM images, exhibiting time-dependent potential fluctuations in the depletion region, as well as local modulations of the junction's boundaries, support our model. These results provide further evidence about the enhanced importance of discrete, individual dopants in the transport mechanism of nanoscale *pn* diodes.

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