Dynamic Evolution Control of Interleaved Boost DC-DC Converter for Fuel Cell Application

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***Abstract*—An electric vehicle powered by the fuel cells called Fuel Cell Electric Vehicles has higher efficiency and lower emissions compared with the internal combustion engine vehicles. In this application, a high power boost dc-dc converter is adopted to adjust the output voltage, current and power of fuel cell engine to meet the vehicle requirements. The major challenge of designing a boost converter for high power application is how to handle the high current at the input and high voltage at the output. In this paper an interleaved boost dc-dc converter is proposed for stepping-up the voltage on high power application. The controller of converter system was designed. A new approach for interleaved boost converter controller based on dynamic evolution control theory is presented. Performance of the interleaved boost converter with the proposed dynamic evolution controller is tested through simulation.**

Keywords-component; Interleaved Boost Converter; Dynamic Evolution Control; Fuel Cell Electric Vehicle; high power application.

I. INTRODUCTION

The use of fuel cells in electric vehicles has received more attention. Fuel cell has higher energy storage capability thus enhancing the range of operation for automobile and is a clean energy source [1-4]. Fuel cells also have the additional advantage of using hydrogen as fuel that will reduce the world dependence on non-renewable hydrocarbon resources [3]. An electric vehicle powered by the fuel cells called Fuel Cell Electric Vehicles (FCEV) has higher efficiency and lower emissions compared with the internal combustion engine vehicles [1]. So, FCEV is providing a much better promising performance [4].

Fig. 1 shows the power supply system of FCEV. The power supply system is composed of Fuel Cell Engine (FCE), Boost DC-DC Converter, energy storage element, and bidirectional dc-dc converter [1-4]. In this system, a high power dc-dc converter is adopted to adjust the output voltage, current and power of FCE to meet the vehicle requirements [2].

Since, the voltage rating of the fuel cells are normally low whereas the motors are driven at higher voltages, a high power and high voltage boost dc-dc converters are needed for providing the interface between the fuel cell energy and high voltage dc-link bus of the inverter [1,2]. In these applications the high power boost converters are required to step up the voltage of FCEV output voltage to the dc-link bus voltage.

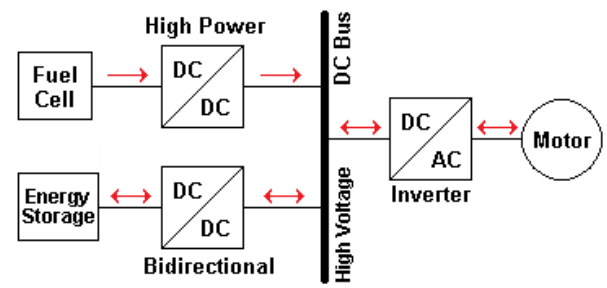

Figure 1. Power supply system of FCEV

In such applications, it becomes a challenge to maintain high efficiency using conventional boost converter. At the same time for high power application like electric vehicle, the low input voltage causes large input current to flow. Also with low duty cycle operation the rms ripple current through the boost diode and output capacitor becomes very high. These increase the losses enormously and make the conventional boost converter quite inefficient. Moreover, parasitic ringing present in practical circuits induces additional voltage stresses and necessitates the use of switches with higher blocking voltage rating, leading to more losses.

The major challenge of designing a boost converter for high power application is how to handle the high current at the input and high voltage at the output [5]. An effective way is to parallel the inputs of the boost converter for input current sharing [5,6]. Based on this concept, an interleaved boost dc-dc converter is a suitable candidate for stepping-up the voltage on high power application [1,2,5-10].

In view of controller, the need for an efficient controller for interleaved boost dc-dc converter is increased [6]. Since boost converter is non-linear time-varying systems, the design of controllers must have capability to cover up the nonlinearity and time-varying properties of the system [4,11].

In this paper, a new approach for interleaved boost converter controller's synthesis, based on dynamic evolution control theory is presented. The proposed dynamic evolution control exploits the non-linearity and time-varying properties of the system to make it a superior controller [1,2]. This control tries to overcome the mentioned problem of linear control by explicitly using dynamic equation model of the converter

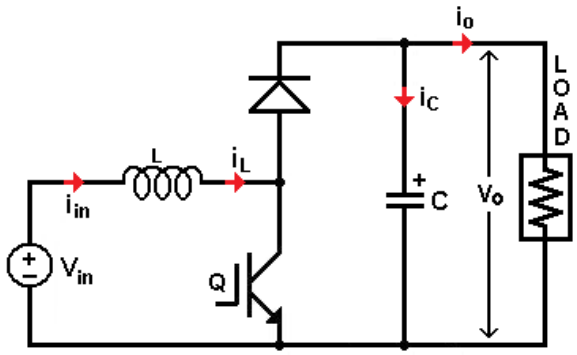

Figure 2. Conventional Boost DC-DC Converter

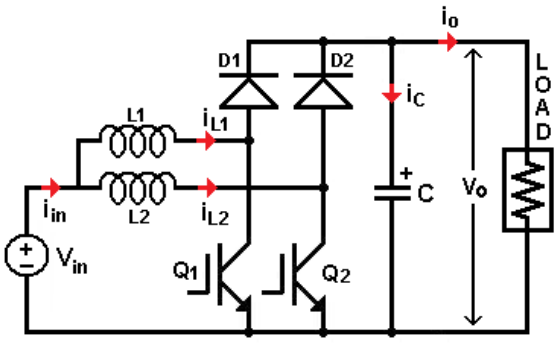

Figure 3. Interleaved Boost DC-DC Converter

for control synthesis [11,12]. Synthesis of dynamic evolution control when applied to boost dc-dc converter is discussed.

A comprehensive simulation analysis was conducted to verify the performance of converter and controller. The performance of dynamic evolution control under step load variation condition is tested through simulation by using MATLAB SIMULINK.

II. BOOST CONVERTER OPERATION

A. Conventional Boost DC-DC Converter

The schematic diagram of the conventional boost dc-dc converter is shown in Fig. 2. The duty cycle, D, is defined as the time relationship that the switch is on relative to the total switching period. Based on the steady state analysis, the DC voltage in the inductor V_L can be expressed as (1) and is equal to zero.

$$V_L = D(V_{in}) - (1-D)(V_{in} - V_O) = 0 \qquad (1)$$

From (1) at steady state it can be verified that the gain ratio between output and input voltage becomes:

$$M = \frac{V_O}{V_{in}} = \frac{D}{1-D} \qquad (2)$$

The inductor current can be obtained by the input and output power:

$$V_{in}.I_L = V_O.I_O$$

$$I_L = \frac{V_O}{V_{in}}.I_O \qquad (3)$$

Substituting (2) into (3), the inductor current can be expressed as:

$$I_L = M.I_O \qquad (4)$$

From (3), the boost converter inductor current will increase proportional to the output power, while (4) says the boost converter inductor current also will increase with the increase of the voltage gain ratio M. These resulted in high inductor

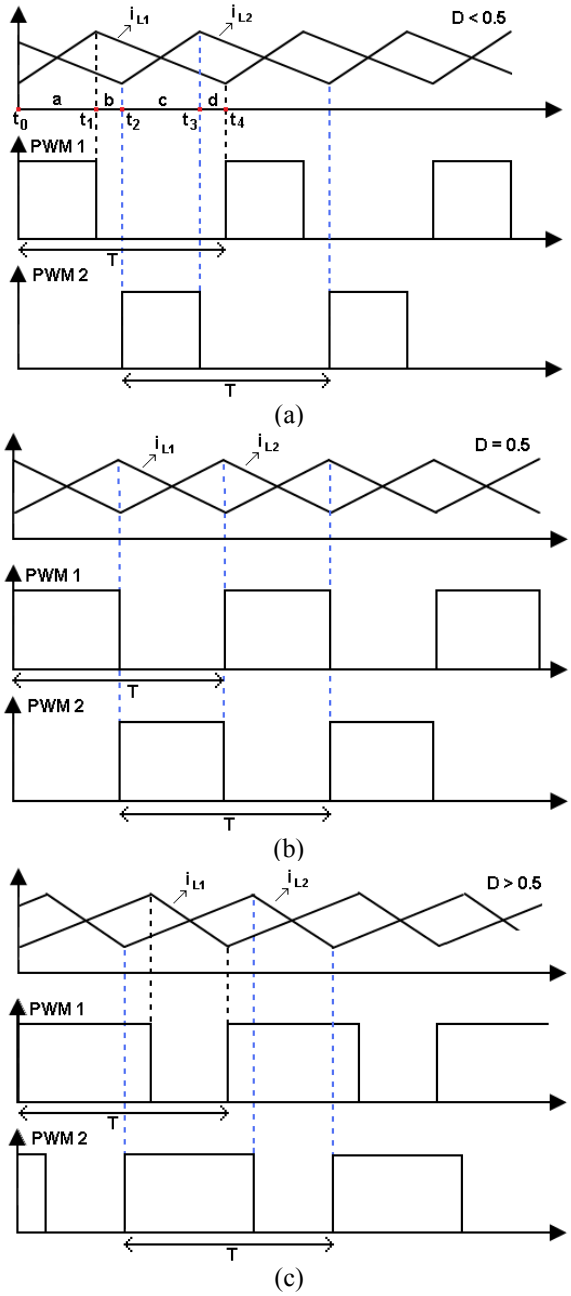

Figure 4. Inductor Current and PWM Signals of Interleaved Boost DC-DC Converter. (a). D < 0.5 (b). D = 0.5 (c). D > 0.5

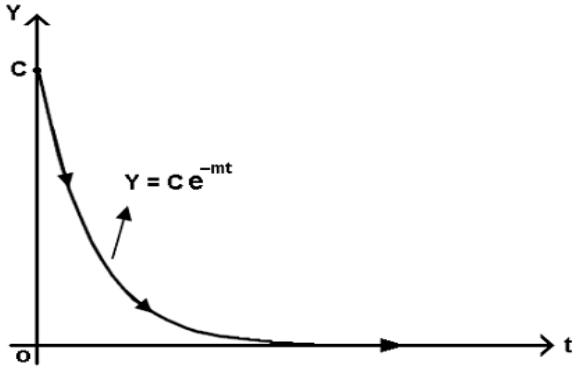

Figure 5. Exponential Evolution Path

currents of boost converter at high power applications. This make the conventional boost converter is quite inefficient for high power applications.

B. Interleaved Boost DC-DC Converter

The interleaved boost dc-dc converter is proposed to deal with the high current problems at high power applications. Fig. 3 shows the schematic diagram of the interleaved boost dc-dc converter, consisting of two parallel connected units, which are controlled by a phase-shifted switching function (interleaved operation).

The interleaved boost dc-dc converter can operate in two modes, continuous current mode (CCM) and discontinuous current mode (DCM). In this paper, the converter is assumed to operate in CCM mode. According to the duty cycle of the PWM pulse (D), the inductor current and PWM signals waveforms of the converter are shown in Fig. 4.

In order to simplify the calculation, it is assumed that the inductance value of both inductor are L_1 and L_2, where L_1=L_2=L, and the duty cycle of Q_1 and Q_2 denoted as $D^1$and D_2, with D_1=D_2=D. According to Fig. 4.a the operations of the CCM modes are explained as follows:

1). State a:

At time t_0, Q_1 is closed and Q_2 is opened. The current of the inductor L_1 starts to rise, while L_2 continues to discharge. The rate of change of i_{L1} is $di_{L1}/dt = V_i/L$, while the rate of change of i_{L2} is $di_{L2}/dt = (V_i - V_o)/L$.

2). State b:

At time t_1, Q_1 and Q_2 are opened. The inductors L_1 and L_2 discharge through the load. The rate of change of i_{L1} and i_{L2} are $di_{L1}/dt = di_{L2}/dt = (V_i - V_o)/L$.

3). State c:

At time t_2, Q_2 is closed while Q_1 still opened. The current of the inductor L_2 starts to rise, while L_1 continues to discharge. The rate of change of i_{L2} is $di_{L2}/dt = V_i/L$, while the rate of change of i_{L1} is $di_{L1}/dt = (V_i - V_o)/L$.

4). State d

At time t_3, Q_2 is opened and Q_1 still opened. The situation is same as state b. The inductors L_1 and L_2 discharge through the load. The rate of change of i_{L1} and i_{L2} are $di_{L1}/dt = di_{L2}/dt = (V_i - V_o)/L$.

Due to the symmetry of the circuit, the next state is similar to the previous.

III. DYNAMIC EVOLUTION CONTROLLER DESIGN

Dynamic evolution Control is a new control technique in power electronics application. The dynamic evolution control has been utilized in reference [3-4], [11] and [12]. The basic idea of the dynamic evolution control is to reduce the error state by forcing the error state to follow the specific path, that ensure the error state goes to zero in increase of time. This specific path is named Dynamic Evolution Path. By using dynamic evolution control, the dynamic characteristic of system is forced to make evolution by following an evolution path.

Design steps of the DEC-based controller can be described in five steps as follows:

1. Evolution path selection.
2. Dynamic evolution function.
3. Analysis of converter system.
4. Synthesis of duty cycle formula.
5. PWM duty cycle generation.

A. Evolution Path Selection

The first step in the DEC-based control design is to determine the evolution path that ensures the error state will go to zero at any increase of time. In this research, the evolution path is an exponential function as shown in Fig. 5. With this evolution path the value of the dynamic characteristic of system will decrease exponentially to zero by equation

$$Y = Y_O.e^{-mt} \tag{5}$$

where, $\boldsymbol{Y}$ is the dynamic characteristic of system, $\boldsymbol{Y_O}$ is the initial value of $\boldsymbol{Y}$, and $\boldsymbol{m}$ is a design parameter specifying the rate of evolution.

B. Dynamic Evolution Function

From (5), the derivative of Y is given as:

$$\frac{dY}{dt} = -m.Yo.e^{-mt}$$

$$\frac{dY}{dt} = -m.Y$$

As a result, the dynamic evolution function of this controller can be written as

$$\frac{dY}{dt} + mY = 0, \qquad \text{m>0} \tag{6}$$

C. Analysis of Converter System

In order to synthesize the control law of the dynamic evolution controller, the dynamic equation of converter system has to be analyzed and substituted into the dynamic evolution function (6).

The controlled converter in this research is the interleaved boost dc-dc converter. Since the interleaved boost converter basically works like two boost dc-dc converter in parallel, then the duty cycle analysis can be performed as a normal boost dc-dc converter.

Based on the state-space average model, the voltage and current dynamics of the boost dc-dc converter are given by

$$v_{in} = L\frac{di_L}{dt} + v_O.\left[1-\alpha\right] \quad (7)$$

where L is the inductance, C the capacitance, v_{in} the input voltage, i_L the inductor current, v_o the output voltage, and α the duty cycle, respectively.

Rearranging (7), the output voltage of converter can be written as:

$$v_O = v_{in} + v_O.\alpha - L\frac{di_L}{dt} \quad (8)$$

D. Synthesis of duty cycle formula

The synthesis of duty cycle formula begins by defining the state error function (***Y***). In this paper, the state error function is a linear function of error voltage as

$$Y = k.v_{err} \quad (9)$$

where k is a positive coefficient, and v_{err} is error voltage.

$$v_{err} = V_{ref} - v_o \quad (10)$$

The derivative of (9) is given by:

$$\frac{dY}{dt} = k.\frac{dv_{err}}{dt} \quad (11)$$

Substitution (9) and (11) into (6), yields

$$k.\frac{dv_{err}}{dt} + m.k.v_{err} \quad (12)$$

$$k.\frac{dv_{err}}{dt} + (m.k-1).v_{err} + V_{ref} = v_o \quad (13)$$

Directly substituting the converter output voltage v_o from (8) into (13) we can get:

$$k.\frac{dv_{err}}{dt} + (m.k-1).v_{err} + V_{ref} = v_{in} + v_O.\alpha - L\frac{di_L}{dt} \quad \text{..... (14)}$$

Solving for α, the obtained duty cycle formula is given by:

$$\alpha = \frac{k.\frac{dv_{err}}{dt} + (m.k-1).v_{err} + L\frac{di_L}{dt} + V_{ref} - v_{in}}{v_O} \quad (15)$$

The expression for duty cycle α is the control action for the converter controller.

Duty cycle formula (15) forces the state error function (***Y***) to satisfy the dynamic evolution function (6). Consequently, the state error function (***Y***) is forced to make evolution by following equation (5) and decrease to zero (***Y*** = 0) with a decrease rate m. So, the state error function (***Y***) satisfy the equation

$$Y = k.v_{err} = 0 \quad (16)$$

Thus the state error of the converter will converge to zero.

$$v_{err} = 0 \quad (17)$$

Substituting (10) into (17), we can see that the voltage output of converter converges to the converters steady state:

$$v_o = V_{ref} \quad (18)$$

From the synthesis procedure, it is clear that the dynamic evolution controller works on the full nonlinear system and does not need any linearization or simplification on the system model at all as is necessary for application of traditional control theory.

Rearranging the duty cycle equation (15), the control law can be written as:

$$\alpha = \frac{V_{ref} - v_{in}}{v_O} + \frac{m.k-1}{v_O}v_{err} + \frac{k}{v_O}\frac{dv_{err}}{dt} + \frac{L}{v_O}\frac{di_L}{dt} \quad (19)$$

It is interesting to note that the control law in (19) consists of four distinct parts. The first part is the feed-forward term, $\frac{V_{ref} - v_{in}}{v_O}$, which is calculated based on the duty cycle at the previous sampling instant. This term compensates for variations in the input voltages. The second and third terms consist of proportional and derivative terms of the perturbations in the output voltage respectively. The last term consists of the derivative terms of the inductor current.

From (19), it is also seen that the input voltage, output voltage and inductor current are involved in control output. The advantage is the dynamic evolution control can compensate all of variation in the input and output voltages also the change of inductor current. It contributes to the better dynamic performance of the controlled system.

E. PWM Duty Cycle Generation

The pwm duty cycle signals are generated by comparing a level control signal with a constant peak repetitive triangle signal (V_{st}). The frequency of the repetitive triangle signal establishes the switching frequency. Since, this frequency is kept constant. Therefore, the dynamic evolution control is operated at constant switching frequency.

Since the interleaved boost converter requires two pwm signals to drive both of switches, the additional work necessary to generate two of pwm signals from single duty cycle formula. Fig. 6 shows the pwm signals generation technique. The first pwm signal is produce when the control signal V_1 is less than V_{st} and the second pwm signal is produce when the control signal V_2 is greater than V_{st}.

The values of the desired level control signals are got from the calculation used the duty cycle formula (15). The values of

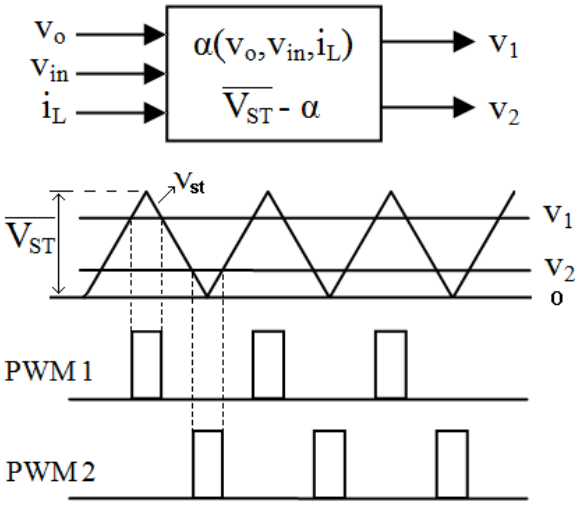

Figure 6. PWM Signal Generation

control signal V_1 and V_2 are given in (20) and (21), while the PWM signals are generated by (22).

$$v_1 = \alpha \tag{20}$$

$$v_2 = \overline{V_{ST}} - \alpha \tag{21}$$

$$\left.\begin{aligned} PWM1 &= v_{st} > v_1 \\ PWM2 &= v_2 > v_{st} \end{aligned}\right\rangle \tag{22}$$

where, V_{st} is the triangle signal and $\overline{V_{ST}}$ is the peak value of V_{st}.

IV. Simulation Results

Based on the analysis above, an interleaved boost dc-dc converter system has been modeled using MATLAB SIMULINK. A comprehensive simulation was conducted to verify the performance of interleaved boost dc-dc converter and controller system.

Fig. 7 illustrated the Simulink model of the interleaved boost dc-dc converter scheme and the dynamic evolution controller. The model parameters are listed in Table I.

The simulation waveform of inteleaved boost dc-dc converter input current, inductor currents and PWM signals are shown in Fig. 8 – 10.

TABLE I.
Simulation Model Parameters

Parameter		Value	Unit
Output Voltage Reference		70	V
Inductor Inductances (L1 & L2)		500	µH
Capacitance (C)		400	µF
Load Resistance		10	Ω
Input Voltage	D < 0.5	50	V
	D = 0.5	35	V
	D > 0.5	20	V

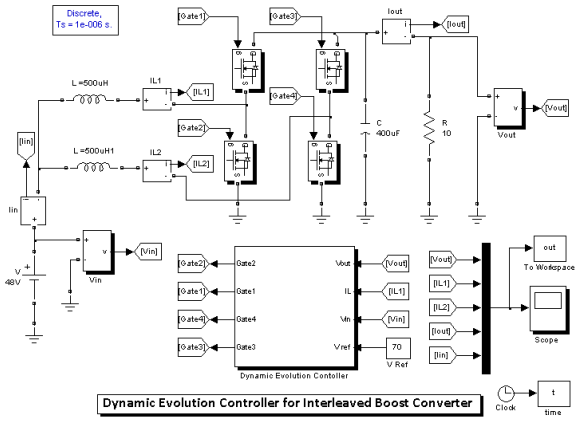

Figure 7. Interleaved Boost Converter Simulation Model

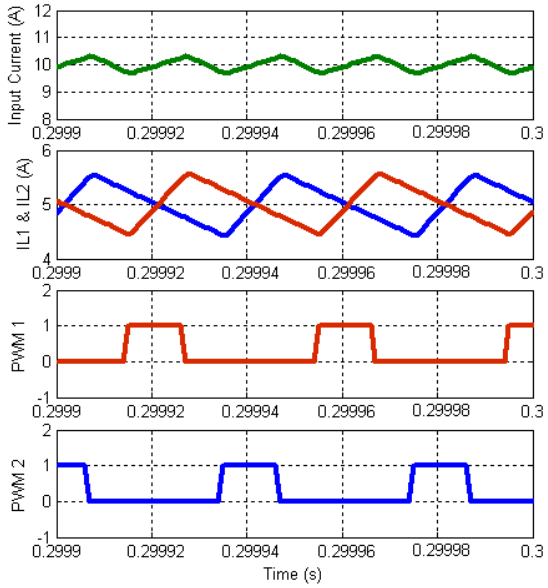

Figure 8. Simulation Result for D < 0.5

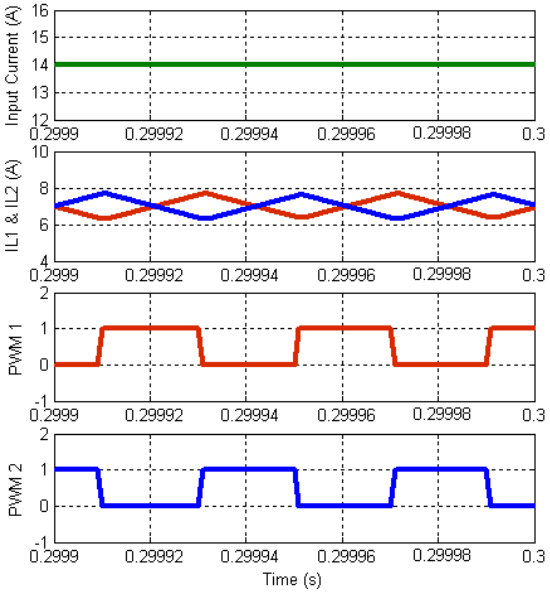

Figure 9. Simulation Result for D = 0.5

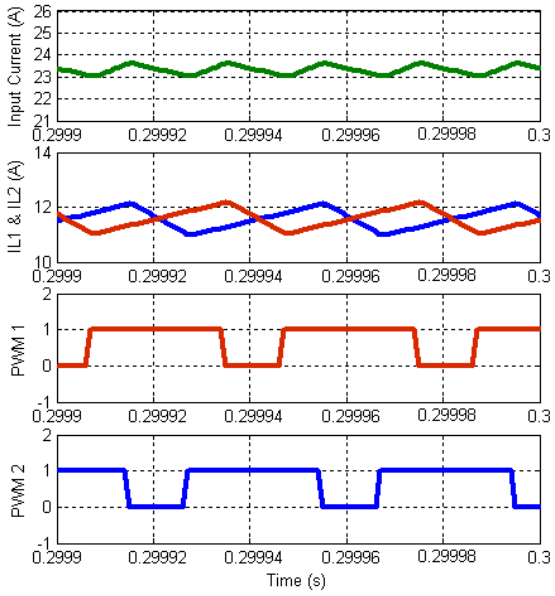

Figure 10. Simulation Result for D > 0.5

A. *PWM Duty Cycle, D < 0.5*

Fig. 8 shows the simulation results for PWM duty cycle, D < 0.5. With a nominal input voltage is 50V, the dynamic evolution controllers manage the output voltage to 70V. In this case, the average duty cycle can be calculated by the equation $D = (V_O - V_i)/V_O$, yielding D = 0.3.

Output current can be calculated by $I_O = V_O/R$, resulting in 7A. Thus, the input current can be estimated through the relationship of $I_{in} = 1/(1 - D) \times I_O$, produces 10A.

B. *PWM Duty Cycle, D = 0.5*

Fig. 9 shows the simulation results for PWM duty cycle, D = 0.5. With a nominal input voltage is 35V, the dynamic evolution controllers manage the output voltage to 70V. In this case, the average duty cycle can be calculated by the equation $D = (V_O - V_i)/V_O$, yielding D = 0.5.

From previous calculation, the output current is 7A. Thus, the estimated input current can be calculated by $I_{in} = 1/(1 - D) \times I_O$, produces 14A.

C. *PWM Duty Cycle, D > 0.5*

Fig. 10 shows the simulation results for PWM duty cycle, D > 0.5. With a nominal input voltage is 20V, the dynamic evolution controllers manage the output voltage to 70V. In this case, the average duty cycle can be calculated by the equation $D = (V_O - V_i)/V_O$, yielding D = 0.7.

The output current is 7A. The average input current is, I_{in} = 23.33A. Simulation results show the input current is devided equally between the two inductor. Therefore, the average inductor currents I_{L1} and I_{L2} are half of input current, ie. $I_{L1} = I_{L2}$ = 11.67A.

CONCLUSION

The dynamic evolution control was proposed for interleaved boost dc-dc converter. The performance of the interleaved boost converter system under various duty cycle condition has been investigated. Simulation results shown the concept of load sharing capability of dynamic evolution controller for 2-cell interleaved boost converter system.

ACKNOWLEDGMENT

The authors would like to thank the Ministry of Science, Technology and Innovation (MOSTI) of the Malaysian government for providing the funding for this research.

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