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Simulation and Implementation of Interleaved Boost DC-DC Converter for Fuel Cell Application

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Abstract

This paper deals with a boost dc-dc converter for fuel cell application. In fuel cell electric vehicles application, a high power boost dc-dc converter is adopted to adjust the output voltage, current and power of fuel cell engine to meet the vehicle requirements. One of challenge in designing a boost converter for high power application is how to handle the high current at the input side. In this paper an interleaved boost dc-dc converter is proposed for current sharing on high power application. Moreover, this converter also reduces the fuel ripple current. Performance of the interleaved boost converter is tested through simulation and experimental results.

***Keywords**: Interleaved Boost Converter, Fuel Cell Electric Vehicle, high power application.*

1. Introduction

The fuel cell is drawing the attention by researchers as one of the most promising power supply in the future. Due to high efficiency, high stability, low energy consumed and friendly to environment, this technology is in the progress to commercialize. Fuel cell has higher energy storage capability thus enhancing the range of operation for automobile and is a clean energy source [1-4]. Fuel cells also have the additional advantage of using hydrogen as fuel that will reduce the world dependence on non-renewable hydrocarbon resources [3]. A Fuel Cell Electric Vehicles (FCEV) has higher efficiency and lower emissions compared with the internal combustion engine vehicles [1]. So, FCEV is providing a much better promising performance [4].

In FCEV application, the power supply system is composed of Fuel Cell Engine (FCE), Boost DC-DC Converter, energy storage element, and bidirectional dc-dc converter [1-4], as show as in Fig. 1. In this system, a high power dc-dc converter is needed to adjust the output voltage, current and power of FCE to meet the vehicle requirements [2].

In such applications, it becomes a challenge to maintain high efficiency using conventional boost converter. At the same time for high power application like electric vehicle, the low input voltage causes large input current to flow. Also with low duty cycle operation the rms ripple current through the boost diode and output capacitor becomes very high. These increase the losses enormously and make the conventional boost converter quite inefficient.

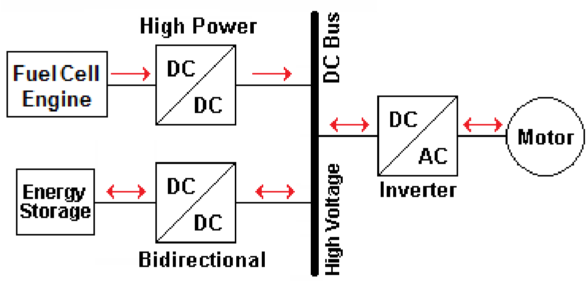

Fig. 1. Power supply system of FCEV

The major challenge of designing a boost converter for high power application is how to handle the high current at the input and high voltage at the output [5]. An interleaved boost dc-dc converter is a suitable candidate for current sharing and stepping up the voltage on high power application [5-10].

In the interleaved boost converter topology, one important operating parameter is called the duty cycle D. For the boost converter, the ideal duty cycle is the ratio of voltage output and input difference with output voltage.

In this paper, a 2-phase interleaved boost converter is considered. As already well known, the input current and output voltage ripple of interleaved boost dc-dc converter can be minimized by virtue of interleaving operation. Moreover, the converter input current can be shared among the phases, which is desirable for heat dissipation. Therefore, the converter reliability and efficiency can be improved significantly.

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In this paper, comprehensive simulation analyses are presented to illustrate the performance of the interleaved boost dc-dc converter. The features of the interleaved boost dc-dc converter, the principle of operation and the design procedure are discussed in this paper. Microcontroller based hardware is developed to verify the performance of the interleaved boost dc-dc converter. The simulation and experimental results are presented and compared.

2. Interleaved Boost converter Operation

Fig. 2 shows the schematic of the dual interleaved boost dc-dc converter. The interleaved boost dc-dc converter consists of two parallel connected boost converter units, which are controlled by a phase-shifted switching function (interleaved operation).

To illustrate interleaving operation, Fig. 3 shows the timing diagram of control signals to the switches. Since this converter has two parallel units, the duty cycle for each unit is equal to (Vout-Vin)/Vout, and it is same for each unit due to parallel configuration. A phase shift should be implemented between the timing signals of the first and the second switch. Since there are two units parallel in this converter, the phase shift value is 180^{O}.

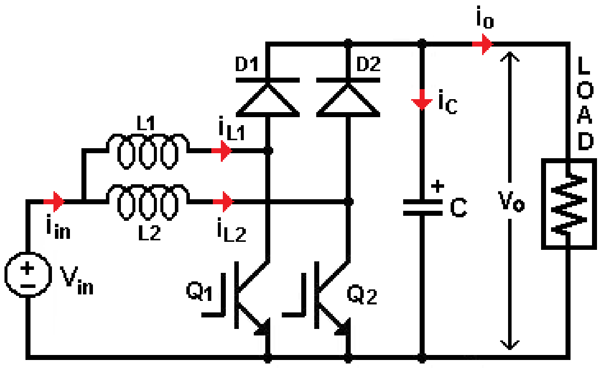

Fig. 2. Interleaved Boost DC-DC Converter

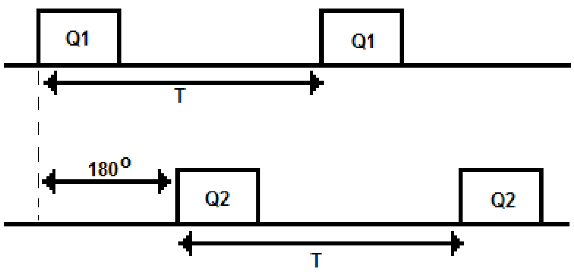

Fig. 3. Timing diagram of Control Signal

The states of operation of this converter are explained as follows. In order to simplify the calculation, it is assumed that the inductance value of both inductor are L_1 and L_2, where L_1=L_2=L, and the duty cycle of Q_1 and Q_2 denoted as $D_1$and D_2, with D_1=D_2=D.

1). State a:

At time t_0, Q_1 is closed and Q_2 is opened. The current of the inductor L_1 starts to rise, while L_2 continues to discharge. The rate of change of i_{Ll} is $di_{Ll}/dt = V_i/L$, while the rate of change of i_{L2} is $di_{L2}/dt = (V_i - V_o)/L$.

2). State b:

At time t_1, Q_1 and Q_2 are opened. The inductors L_1 and L_2 discharge through the load. The rate of change of i_{Ll} and i_{L2} are $di_{Ll}/dt = di_{L2}/dt = (V_i - V_o)/L$.

3). State c:

At time t_2, Q_2 is closed while Q_1 still opened. The current of the inductor L_2 starts to rise, while L_1 continues to discharge. The rate of change of i_{L2} is $di_{L2}/dt = V_i/L$, while the rate of change of i_{L1} is $di_{L1}/dt = (V_i - V_o)/L$.

4). State d:

At time t_3, Q_2 is opened and Q_1 still opened. The situation is same as state b. The inductors L_1 and L_2 discharge through the load. The rate of change of i_{Ll} and i_{L2} are $di_{Ll}/dt = di_{L2}/dt = (V_i - V_o)/L$.

Due to the symmetry of the circuit, the next state is similar to the previous.

3. PWM Signals Generation Technique

The pwm duty cycle signals are generated by comparing a level control signal (Vc) with a constant peak repetitive triangle signal (Vst). The frequency of the repetitive triangle signal establishes the switching frequency. Since the interleaved boost converter requires two pwm signals to drive both of switches, the additional work necessary to generate two of pwm signals from single duty cycle formula. Fig. 4 shows the pwm signals generation technique. The first pwm signal is produce when the control signal V_1 is less than V_{st} and the second pwm signal is produce when the control signal V_2 is greater than V_{st}.

The value of the desired level control signal (V_c) is got from controller output. The values of control signal V_1 and V_2 are given in (1) and (2), while the PWM signals are generated by (3).

$$v_1 = v_c \quad (1)$$

$$v_2 = \overline{V_{ST}} - v_c \quad (2)$$

$$\begin{aligned} PWM1 &= v_{st} > v_1 \\ PWM2 &= v_2 > v_{st} \end{aligned} \quad (3)$$

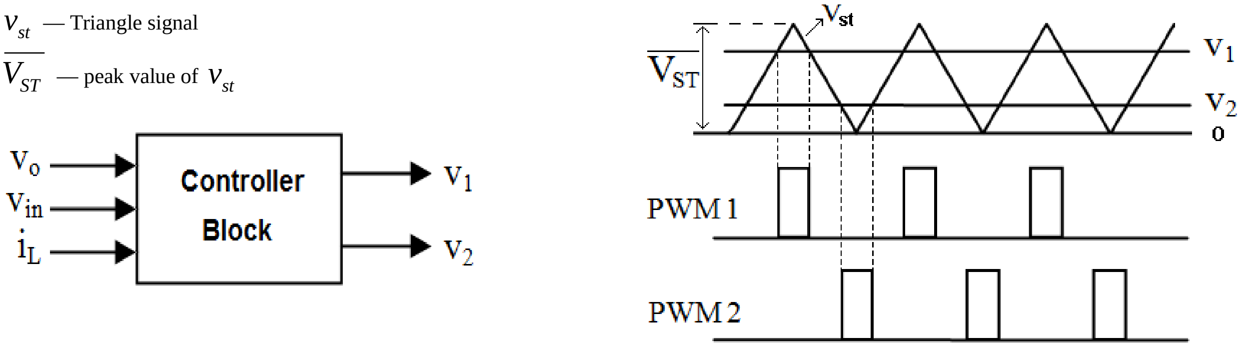

Fig. 4. PWM Signal Generation

4. Simulink Model and Simulation

An interleaved boost dc-dc converter system has been modeled using MATLAB SIMULINK. A comprehensive simulation was conducted to verify the performance of interleaved boost dc-dc converter system. Fig. 5 illustrated the Simulink model of the interleaved boost dc-dc converter scheme. The model parameters are listed in Table 1. The simulation waveform of inteleaved boost dc-dc converter input current, inductor currents and PWM signals are shown in Fig. 6 – 8.

Table 1. Simulation Model Parameters

Parameter		Value	Unit
Output Voltage Reference		70	V
Inductor Inductances (L1 & L2)		500	μH
Capacitance (C)		400	μF
Load Resistance		10	Ω
Input Voltage	D < 0.5	50	V
	D = 0.5	35	V
	D > 0.5	20	V

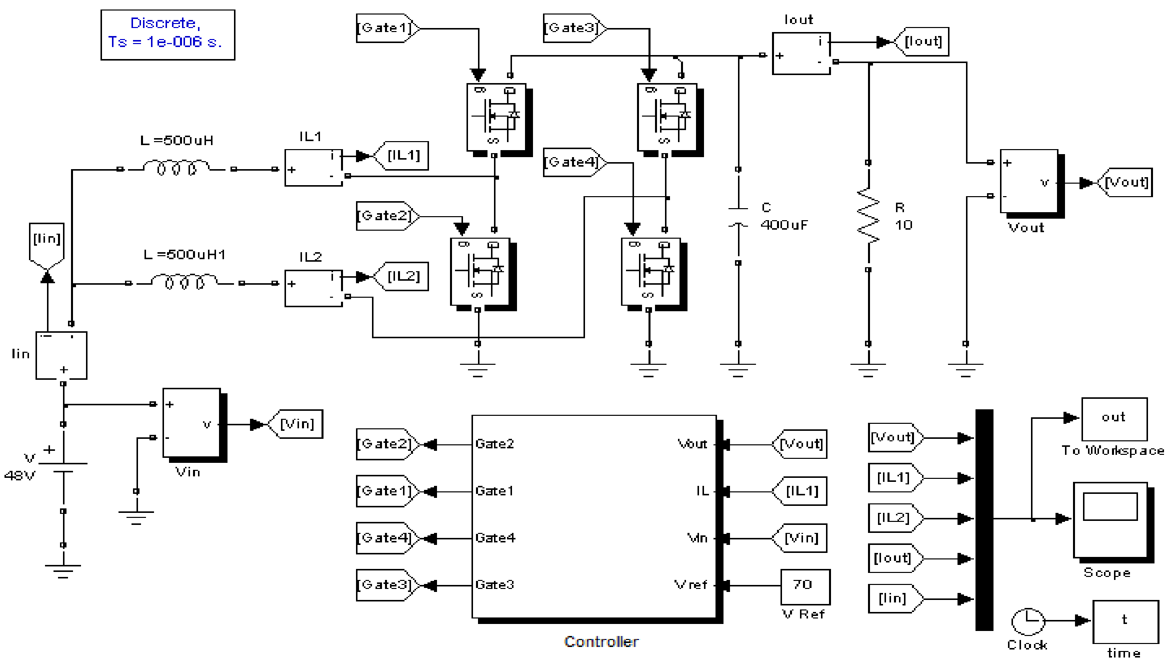

Fig. 5. Interleaved Boost Converter Simulation Model

A. *PWM Duty Cycle, D < 0.5*

Fig. 6 shows the simulation results for PWM duty cycle, D < 0.5. With a nominal input voltage is 50V, the controllers manage the output voltage to 70V. In this case, the average duty cycle can be calculated by the equation $D = (V_O – V_i)/V_O$, yielding D = 0.3. Output current can be calculated by $I_O = V_O/R$, resulting in 7A. Thus, the input current can be estimated through the relationship of $I_{in} = 1/(1 – D) \times I_O$, produces 10A.

B. *PWM Duty Cycle, D = 0.5*

Fig. 7 shows the simulation results for PWM duty cycle, D = 0.5. With a nominal input voltage is 35V, the controllers manage the output voltage to 70V. In this case, the average duty cycle can be calculated by the equation $D = (V_O – V_i)/V_O$, yielding D = 0.5. From previous calculation, the output current is 7A. Thus, the estimated input current can be calculated by $I_{in} = 1/(1 – D) \times I_O$, produces 14A.

C. *PWM Duty Cycle, D > 0.5*

Fig. 8 shows the simulation results for PWM duty cycle, D > 0.5. With a nominal input voltage is 20V, the controllers manage the output voltage to 70V. In this case, the average duty cycle can be calculated by the equation $D = (V_O – V_i)/V_O$, yielding D = 0.7.

The output current is 7A. The average input current is, I_{in} = 23.33A. Simulation results show the input current is devided equally between the two inductor. Therefore, the average inductor currents I_{L1} and I_{L2} are half of input current, ie. $I_{L1} = I_{L2}$ = 11.67A.

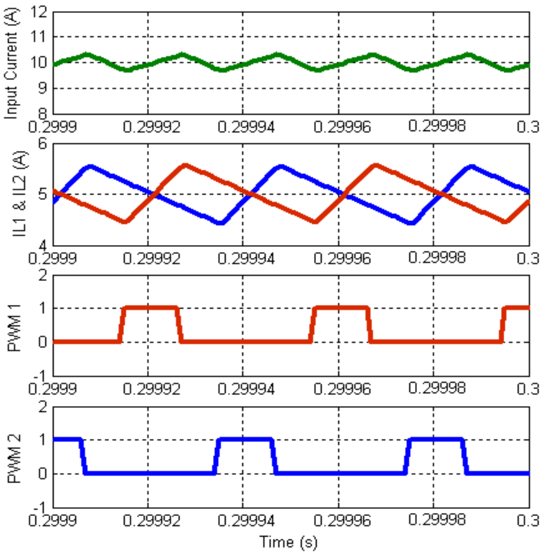

Fig. 6. Simulation Result for D < 0.5

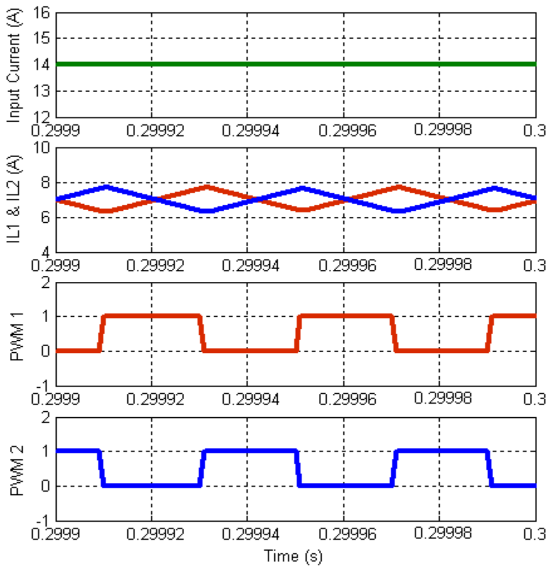

Fig. 7. Simulation Result for D = 0.5

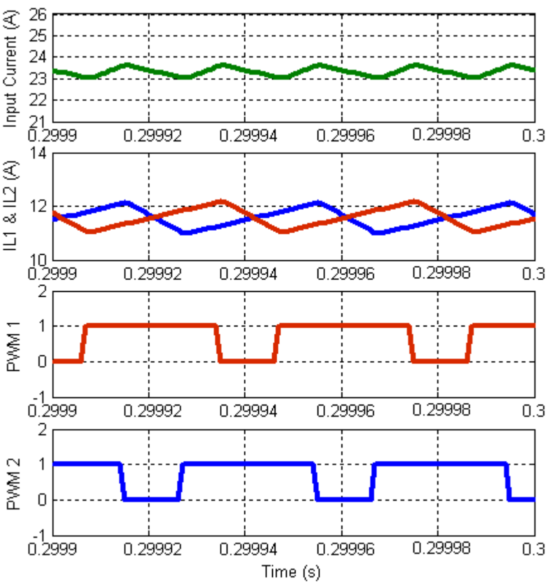

Fig. 8.Simulation Result for D > 0.5

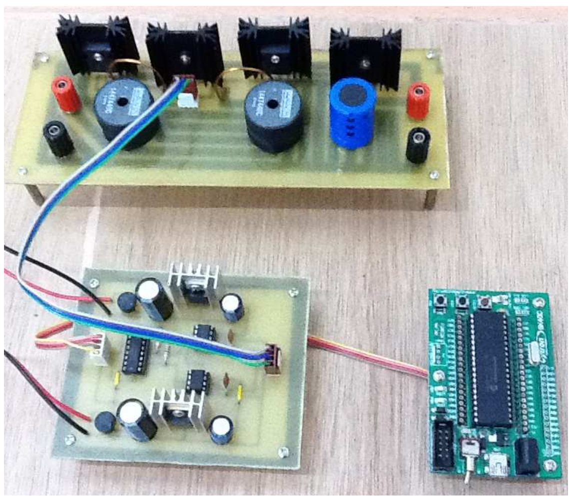
Fig. 9. Hardware prototype of the interleaved boost dc-dc converter

5. Hardware Prototype and Experiment Results

In order to validate the actual performance of the presented interleaved boost dc-dc converter, a hardware prototype was designed and built. Fig. 9 shows the hardware prototype of the interleaved boost dc-dc converter. Each switch in this interleaved boost dc-dc converter is running at 20 khz switching frequency. In this work, the prototype have three of main circuit part. The First circuit is the power circuit. The power circuit build using two of power IGBT HGTG20N60B, two of ultra fast diode 60EPU04P, two of 470mH power inductor and 100 uF electrolyte capacitor. The second circuit is the gate drive circuit. The HCPL 3120 gate drive IC is choose as the gate driver in this work. Two of HCPL 3120 IC are used to drive both of Power IGBT. The last but not less is the controller circuit. The Microchip PIC 16F877A microcontroller is use as the main controller. The PIC 16F877A have 8 ADC input onchip and two PWM output.

The experiment results of the implemented inteleaved boost dc-dc converter input current, inductor currents and PWM signals are shown in Fig. 10 – 12. Fig. 10 shows the experiment results for PWM duty cycle, D < 0.5. The nominal input voltage is 50V, the output voltage is 70V. The calculated average duty cycle D = 0.3. Fig. 11 shows the experiment results for PWM duty cycle, D = 0.5. The nominal input voltage is 35V, the output voltage is 70V. The calculated average duty cycle D = 0.5. Fig. 12 shows the experiment results for PWM duty cycle, D > 0.5. The nominal input voltage is 20V, the output voltage is 70V. The calculated average duty cycle D = 0.7.

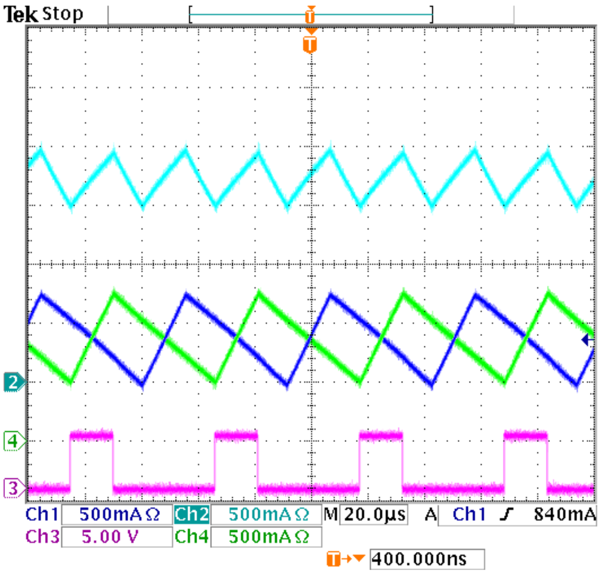

Fig. 10. Experiment Results for D = 0.3

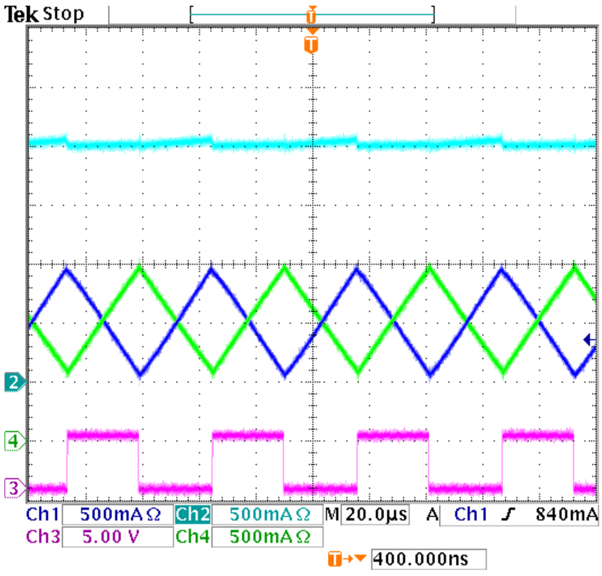

Fig. 11. Experiment Results for D = 0.5

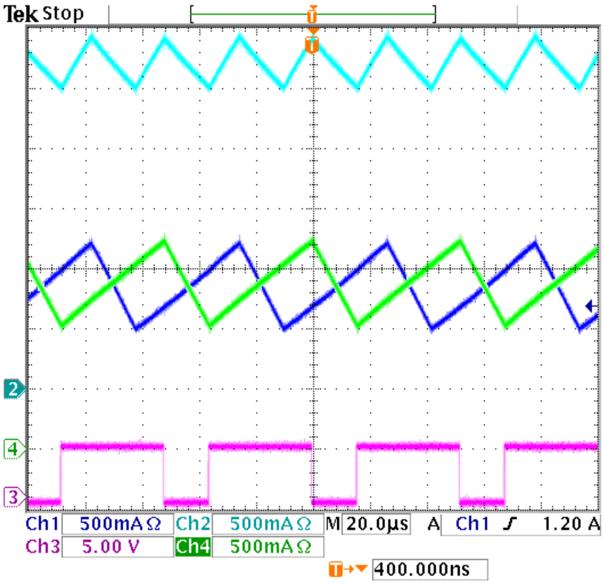

Fig. 12. Experiment Results for D = 0.7

6. Conclusion

In This Paper, a simulation and hardware implementation of the dual interleaved boost dc-dc converter was presented. The feature and performance of the interleaved boost converter system under various duty cycle condition has been investigated. Simulation and experimental results shown that the interleaved boost converter have the ability for input current sharing as well as reducing the ripple input current.

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