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SPEED CONTROL OF PERMANENT MAGNET SYNCHRONOUS MOTOR USING FPGA FOR HIGH FREQUENCY SIC MOSFET INVERTER

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Abstract

This paper proposes a digital hardware control of Permanent Magnet Synchronous Motor (PMSM) using a SiC MOSFET inverter implemented in a FPGA (Field Programmable Gate Array) device. High frequency is required using a SiC MOSFET inverter to obtain high response and good stability for speed control systems. Not only the switching frequency of inverter, but also the control frequency is achieved up to 100 kHz for speed control system of AC motor drive including vector control and dq transformation. As the result, high response control system of PMSM can be achieved. Digital hardware control based on FPGA is used to maximize the switching frequency of SiC MOSFET inverter. Finally, an experimental system is set up and some experimental results are demonstrated.

Keywords: Speed control, High frequency, SiC MOSFET inverter, FPGA, PMSM.

1. Introduction

This paper presents a new speed control system of permanent magnet synchronous motor (PMSM) using FPGA (Field Programmable Gate Array) with an SiC inverter. SiC MOSFET is one of the most promising alternatives to Silicon (Si) for power semiconductor devices due to its superior material characteristics. SiC devices provide significant performance improvement compared to traditional Si devices, such as lower conduction loss and higher switching speed [1]. SiC is a compound semiconductor comprised of Silicon (Si) and Carbon (C). The inverter using SiC MOSFET is presented to achieve high-frequency operation up to 100 kHz with a switching PWM technique.

Nomenclatures

D_v	Viscous damping coefficient, N.m/rad/s
I_d	Direct axis current, A
I_q	Quadrature axis current, A
J	Moment inertia of motor, kg.m^2
k_t	Torque coefficient, N.m/A
L_a	Armature' self- inductance, H
P	d/dt
R_a	Armature resistance, Ohm
T_e	Electromagnetic torque, N.m
T_L	Load torque, N.m
v_d	Direct axis voltage, V
v_q	Quadrature axis voltage, V

Greek Symbols

λ	Number of pole pairs of motor
Φ_a	Armature flux, Wb
Φ_m	Maximum magnetic flux, Wb
ω	Motor angular speed, rad/s
ω_m	Mechanical angular speed, rad/s
ω_{re}	Electrical angular speed, rad/s

PMSM has been widely used in many industrial applications such as robots, rolling mills and machine tools [2]. PMSM has advantages like high efficiency, high power factor, high power density and maintenance free operation, and this motor is nowadays preferred in a variety of applications [3].

A high-performance motor control system requires a high response system and recovery to steady state condition immediately when a motor is loaded and influenced by any disturbances. To achieve it, the high frequency PWM is needed so the speed control system using FPGA with SiC inverter is proposed. There are many advantages of using high frequency PWM (in range of 50 to 100 kHz) in motor drive applications. High motor efficiency, fast control response, lower motor torque ripple, close to ideal sinusoidal motor current waveform, smaller filter size, lower cost filter, etc. are a few of the advantages [4].

There are many published studies that have given attention to achieve a high response control system in the speed control of a permanent magnet synchronous motor. Zhou [5] proposed an FPGA-realisation of a speed servo controller of PMSM. Ying [6] proposed a speed control integrated circuit (IC) for permanent magnet synchronous motor (PMSM) drive under this SoPC environment. Then, an adaptive fuzzy controller is adopted to cope with the dynamic uncertainty and external load effect in the speed loop of PMSM drive.

Hanamoto [7] proposed the hardware speed control system of PMSM using FPGA. However, the above researches studied the speed control system on Si based inverter and achieved the frequency of PWM in the 20-40 kHz range. Kamel [2] and Advan [3] proposed speed control of PMSM using Fuzzy Logic Controller. These researches used simulation with MATLAB SIMULINK to perform Fuzzy Logic Controller in the speed control of permanent magnet synchronous motor.

This paper proposes the use of SiC MOSFET based inverter in the speed control of permanent magnet synchronous motor. High response system is achieved by using SiC MOSFET in this research so that the motor can recover to steady state value as soon as possible. It takes only 0.02 s to reach the steady state value. Because the processing speed gets faster, software control principally has a calculation time limitation. FPGA is used for speed and torque control because high speed calculation is obtained using the ability of the hardware processing [7].

2. Mathematical Model of PMSM

Voltage equations of PMSM are derived in two-axis *d-q* synchronous rotating reference frame, as in equation (1) [8]

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} R_a + PL_a & -\omega_{re}L_a \\ \omega_{re}L_a & R_a + PL_a \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 0 \\ \omega\phi_m \end{bmatrix} \quad (1)$$

where v_d and v_q are direct and quadrature axis voltages; i_d and i_q are direct and quadrature axis currents; R_a is armature resistance; L_a is armature' self-inductance; ω_{re} is the electrical angular speed; Φ_m is maximum magnetic flux; P is d/dt. The electromagnetic torque can be simplified to equation (2).

$$T_e = \lambda\Phi_a i_q = k_t i_q \quad (2)$$

where λ is the number of pole pairs of motor; Φ_a is armature flux; k_t is torque coefficient; i_q is q axis current. The dynamic equation of PMSM can be written as in equation (3).

$$J\frac{d\omega_m}{dt} + D_v = T_e - T_L \quad (3)$$

where J is moment inertia of the motor; D_v is viscous damping coefficient; T_e and T_L are electromagnetic torque and load torque where ω_m is mechanical angular speed.

3. SiC MOSFET Inverter

SiC devices such as MOSFETs offer the benefit of efficient power conversion in areas that current Si-based power semiconductors do not [9]. The inverter presented in this paper is designed by using SiC MOSFET for switching component and Schottky Barrier Diode (SBD) is connected in parallel with each SiC MOSFET to reduce the switching loss and specifically the reverse recovery loss [10]. SBD offers a number of advantages such as low turn on voltage, fast recovery time, and low junction capacitance. The inverter topology is shown in Fig. 1.

Pulse Width Modulation (PWM) method is used for switching of inverter. There are 8 switching modes of inverter. The combined voltage vector in each mode is shown in Fig. 2. Each resultant vector has a phase difference of $2\pi/3$ from each other. The inverter's switching modes are shown in Table 1. The load side of the same voltage by turning ON simultaneously the switching elements of the DC negative voltage side or the DC positive voltage side, V_0 or V_7 is zero voltage.

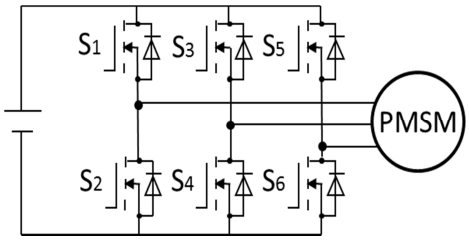


Fig. 1. Inverter Circuit.

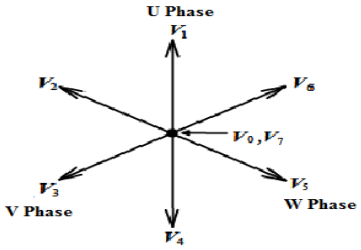


Fig. 2. Voltage Vector.

Table 1. Switching Modes of Inverter.

Mode	U Phase	V Phase	W Phase	Vector Resultant
0	S_2	S_4	S_6	V_0
1	S_1	S_4	S_6	V_1
2	S_1	S_3	S_6	V_2
3	S_2	S_3	S_6	V_3
4	S_2	S_3	S_5	V_4
5	S_2	S_4	S_5	V_5
6	S_1	S_4	S_5	V_6
7	S_1	S_3	S_5	V_7

The carrier wave comparison method is used to generate a PWM pulse. A carrier wave is shown in Fig. 3. A carrier wave is made by counting up/down counter (200 MHz). The circuit generating carrier wave is shown in Fig. 4. There are 1000 up/down counters implemented in FPGA. A control period is synchronised every half cycle. In this research, frequency of PWM is 100 kHz and control frequency is 200 kHz.

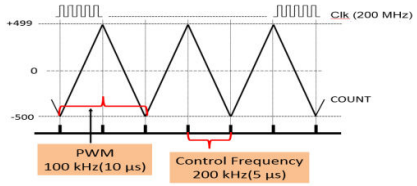


Fig. 3. Carrier Wave.

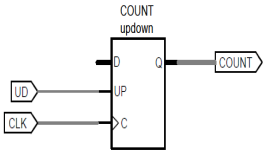


Fig. 4. Carrier Wave Circuit.

4. Digital Hardware Control of Permanent Magnet Synchronous Motor

The control method of PMSM is a vector control employed for variable speed control systems. The speed commands are sent to control blocks which include three PI controllers for speed control and two current control loops, dq and inverse dq coordinate transformation. Then, a PWM pulse generator is produced for switching of inverter. Rotor position and motor angular speed are detected and calculated from a pulse series generated from an incremental pulse encoder which is mounted on the rotor axis of the PMSM.

Phase currents are measured by sensors and converted into a digital value by 12 bit AD converters. In order to maximize the switching frequency, a high

performance FPGA based digital hardware controller is used to implement the speed control of a permanent magnet synchronous motor. FPGA is used for the torque and speed control in some cases because a fast processing operation is obtained using the ability of the hardware processing.

Figure 5 shows a proposed digital hardware control system for the speed control system of PMSM by using FPGA. FPGA (XILINX Spartan3E XC3S1600E) is used to control the speed control of PMSM.

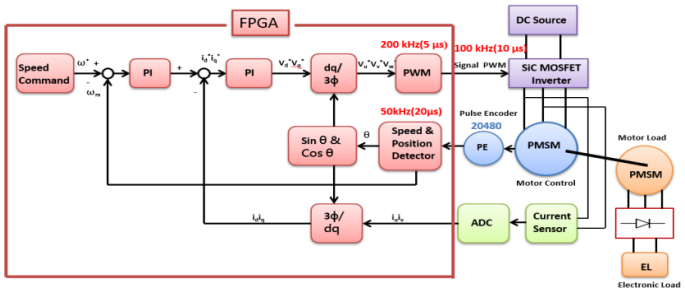


Fig. 5. Speed Control of PMSM Block Diagram of the Proposed System.

Program algorithm is written in VHDL [11]. VHDL is a hardware description language that describes the behaviour of an electronic circuit or system, from which the physical circuit or system can be implemented. Multipliers, adder, and subtraction are employed for the calculation. A timing generator is used to generate timing of operation. It also generates a control signal, sampling signal of Analog to Digital Converter and speed detector. The signals connect to modules and manage the control period, sampling period of encoder and input/output data timing of the peripheral device.

Figure 6 shows speed and position detector circuits implemented in the FPGA which consists of a counter, latch and multiplier. The speed should be the same units as the speed command value of the speed command block. The speed sampling pulse that indicates the speed detection circuit is a signal generated by the timing generator. Rotor position θ is obtained using an Up/Down counter. In the FPGA sin θ/cos θ can be obtained by using a look-up table.

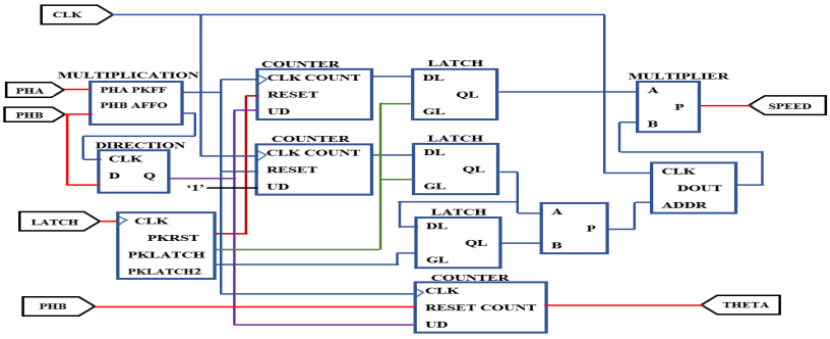


Fig. 6. Speed and Position Detector Circuit.

There are three PI (Proportional Integral) controllers used for both speed and current control. In the PI controller, each variable has a 32 bit data to keep precision. Figure 7 shows the hardware system of a PI speed controller which consists of shift register, latch, subtraction, adder and multiplier. Calculation of the PI speed controller circuit is performed in the order of timing calculation provided by the shift register. Deviation of the measured value with the command value is taken by the first subtraction. Deviation is latched in each control cycle by the calculation timing which is multiplied by the gain at the next timing. The accumulator is a circuit which performs an integration operation.

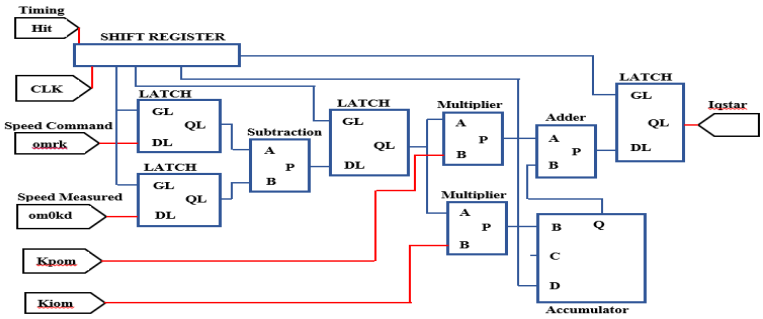


Fig. 7. PI Speed Controller Circuit.

The current detector circuit is used to create a signal for controlling the AD converter. It is necessary to provide adequate signal to each pin of the AD converter. It is also necessary to create a current signal using a 1 bit data to perform serial communication using an AD converter. Figure 8 shows a time chart of the AD converter operation. AD conversion is begun in accordance with the rising edge of the CS signal. Therefore, it is necessary to capture the output signal of the AD converter at the rising edge of the CLK. A current 12 bit signal is created by using a 12 bit shift register. The detail of the signals is shown in Table 2.

Figure 9 shows the design of a current detector which consists of a D flip-flop, shift register and counter. The signal from the current detector circuit will be sent to the AD converter. The timing (Hit) is used for the timing generation circuit, and converted into 12 bit shift register parallel signals. Figure 10 shows a dq coordinate transformation circuit. The operation of the dq coordinate transformation is to convert uvw coordinates into αβ coordinates and convert αβ coordinates into dq coordinates. Phase currents are converted to dq axis for space vector control. Interface used in this research is shown in Fig. 11.

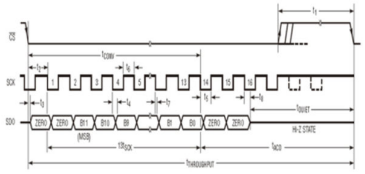


Fig. 8. Time Chart for A/D Converter.

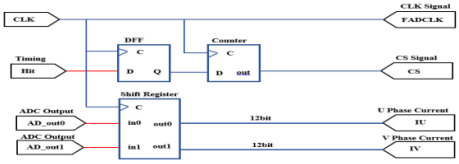


Fig. 9. Current Detector Circuit.

Table 2. Signal Timing Characteristics.

Input and Output Signal of AD Converter		
CS	Start of conversion to digital values from the analog value	Signal of conversion start
SCK	CLK signal is sent to the AD converter	Clock Signal
SDO	1 bit Data is sent from the AD Converter	Output Signal
Timing Characteristic of Signal		
t_1	Minimum Positive or Negative CS Pulse Width	4 ns Min
t_2	Setup Time After CS ↓	6-2000 ns
t_3	SDO Enabled Time After CS ↓	4 ns Max
t_4	SDO Data Valid Access Time After SCK ↓	15 ns Max
t_5	SCK Low Time	40%(t_{SCLK}) Min
t_6	SCK High Time	40%(t_{SCLK}) Min
t_7	SDO Data Valid Hold Time After SCK ↓	5ns Min
t_8	SDO Into Hi-Z State Time After SCK ↓	5-14 ns
t_9	SDO Into Hi-Z State Time After CS ↑	4.2 ns Max
t_{SCK}	Shift Clock Frequency	0.5-48 MHz
$t_{THROUGHPUT}$	Minimum Throughput Time， tACQ + tCONV	333 ns Max
t_{CONV}	Conversion Time	277 ns Min
t_{ACQ}	Acquisition Time	56 ns Min
t_{QUIET}	SDO Hi-Z State to CS ↓	4 ns Min

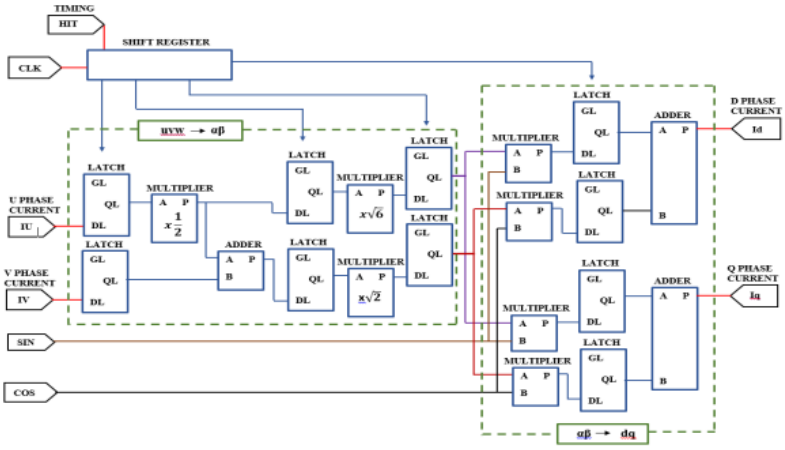


Fig. 10. dq Coordinate Transformation Circuit.

The current sensor is connected to interface and converted into a digital value by an ADC. Signal from an incremental pulse encoder is connected to signal from encoder side. The output side is connected to a data recorder (HIOKI Memory Hicorder) for checking data through a DA converter. Table 3 shows the specification of the FPGA used in the system.

Table 3. Specification of FPGA XC3S1600E-4FG320 Using in the System.

Logic Utilisation	Used	Available	Utilisation
Total No. Slice Registers	1775	29504	6%
Number of Occupied Slices	2730	14752	18%
Total Number of 4 input LUTs	4635	29504	15%
Number of bonded IOBs	26	250	10%
Number of Block RAM	33	36	91%
Number BUFGMUXs	14	24	58%
Number of DCMs	2	8	25%

5. Experimental and Result

5.1. Experimental setup

The proposed experimental system is depicted in Fig. 12 and the PMSMs used for experiment are shown in Fig. 13. Two types of PMSMs are used for the control system, one is for the motor and the other is for the load. Both of them are connected via coupling. Encoder is mounted on the rotor axis of the PMSM. The FPGA used for experiment is shown in Fig. 11.

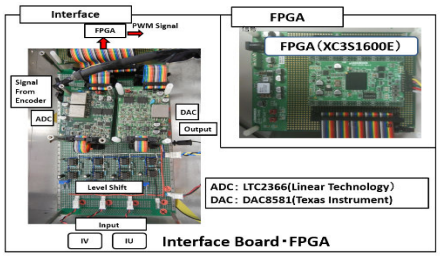


Fig. 11. FPGA and Interface.

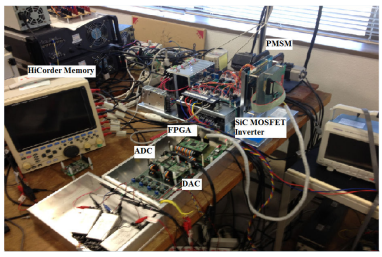
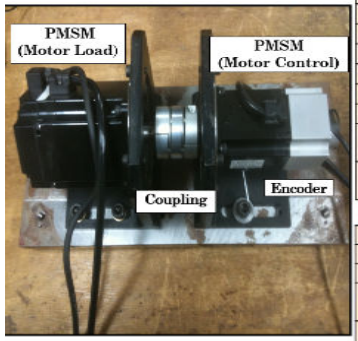


Fig. 12. Experimental Apparatus.



Permanent Magnet Synchronous Motor

Motor Control Specification

Model	SGMAS04A		
Manufacturing	Yaskawa		
Item	Symbol	Unit	Value
Power	P_R	W	400
Speed	N_R	min^{-1}	3000
Torque	T_R	N m	1.27
Inertia	J_M	kg m^2	0.19×10^{-4}
Current	I_R	A	2.6
Torque constant	Kt	N m/A(rms)	0.527
Armature Resistance	Ra	Ω	1.56
Armature Inductance	La	mL	3.82

Motor Load Specification

Model	SGMJV-08ADA21		
Manufacturing	Yaskawa		
Item	Symbol	Unit	Value
Inertia	J_M	kg m^2	1.57×10^{-4}
Torque constant	Kt	N m/A(rms)	0.119
Armature Resistance	Ra	Ω	0.541
Armature Inductance	La	mH	2.24

Fig. 13. Permanent Magnet Synchronous Motor.

5.2. Experimental result

Figure 14 shows the PWM for switching of an inverter seen on the screen of an oscilloscope. 100 kHz is achieved using FPGA. FPGA is the best way of designing a digital PWM generator. Time resolution is 10 ns. *U*, *V*, and *W* phases are seen on the screen for each positive and negative value. Each phase has a phase difference of $2\pi/3$ from each other. Furthermore, PWM has a dead time processing for delaying between the gating signals of the top and bottom devices in an inverter leg to prevent a short circuit of a DC link. 0.5 µs dead time is achieved using FPGA.

Figure 15 shows a step response of the proposed system. The speed command is changed from 100 min^{-1} to 150 min^{-1}. The speed decreases when the motor is loaded and recovered to the steady state condition immediately. It takes only 0.02 s to reach the steady state value. The q-axis current is equivalent to the motor torque and the current increases when the motor is loaded. The results are obtained by using a clock frequency of FPGA which is set to 48 MHz and encoder pulse is 20480 ppr. The PWM switching frequency is achieved up to 100 kHz. The control frequency is achieved up to 200 kHz and only when the frequency of a speed detector is 50 kHz. Experimental results show the feasibility of a high performance system of PMSM speed control system using FPGA.

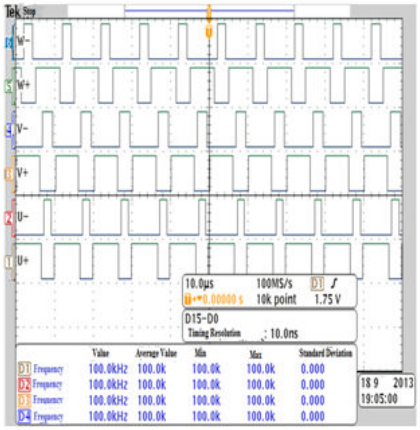


Fig. 14. Pulse Width Modulation.

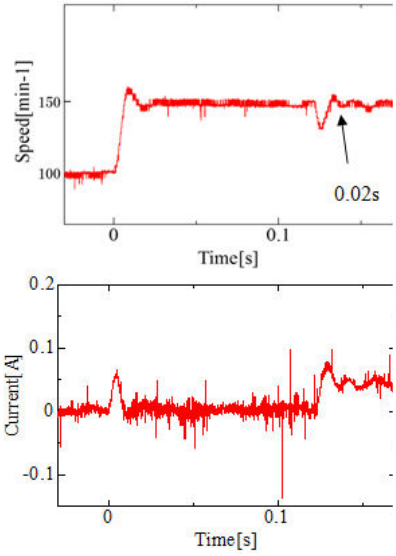


Fig. 15. Step Response of a Proposed Speed Control System.

6. Conclusions

The use of a SiC MOSFET in an inverter for speed control of PMSM based on FPGA has been proposed and verified with experimental results. Experimental results show the superiority of a SiC MOSFET where the switching frequency can be achieved up to 100 kHz. Digital hardware control systems using FPGA work well for achieving

the switching frequency of an inverter up to 100 kHz. FPGA can be used to ensure fast processing operation in a high frequency switching of an inverter.

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