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Penulis,

Megetahui,
Dekan Fakultas Teknik Unila

Prof. Ir. Suharno, M.Sc., Ph.D., IPU.
NIP. 196207171987031002

Dr. Eng. Helmy Fitriawan, S.T., M.Sc.
NIP. 197509282001121002

Menyetujui,
Ketua LPPM Universitas Lampung

Dr. Ir. Lusmeilia Afriani, D.E.A.
NIP. 196505101993032008

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Welcome messages

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Ministry of Research, Technology and Higher Education

Dear participants, guests ladies and gentlemen. It is both a great pleasure and honor to welcome you all at the 2016 IEEE International Symposium on Electronics and Smart Devices (ISESD), here in Mercure Bandung Setiabudi, Bandung, Indonesia.

The Directorate General of Institutional Affairs currently puts a lot of efforts to increase the level of universities in Indonesia to a World Class University level. In correspond to these efforts, we hold a national center of excellence program. This program covers topics that are essential to the development of Indonesia. As a part of the National Center of Excellence (CoE), Microelectronics Center is one research center that is supported by us to be the leader in microelectronics area. In the national level, besides microelectronics center, we have other 19 CoEs. This is a prestigious and very competitive program for all univesities in Indonesia.

As a national research center, we also give them a mandate to hold an international conference. We hope that by holding such an event, they can expose their research result, can communicate with many experts from all around the world, and can contribute to the society. We also hope that this conference will be a periodical conference that involves many experts and can be held in different places in Indonesia.

Finally, we would like to express our sincere gratitude to the Insitut Teknologi Bandung (ITB) and Microelectronics Centers ITB and all the technical sponsors for their excellent supports in this conference. We hope that the gathering of ISESD 2016 participants from various countries and cultures will bring a better understanding from each other and all of you will have enjoyable time here in Bandung, Indonesia.

Welcome messages

Dr. Ir. Kadarsah Suryadi, DEA
Rector
Institut Teknologi Bandung, Indonesia

Dear participants, guests ladies and gentlemen. It is both a great pleasure and honor to welcome you all at the 2016 IEEE International Symposium on Electronics and Smart Devices (ISESD), here in Mercure Setiabudi Bandung, Bandung, Indonesia.

Institut Teknologi Bandung (ITB) has been known as a leading university in the field of science and technology in Indonesia. There are many works from the alumnee that give a significant contribution to the development of Indonesia through the use of technology. ITB as a university, should always follows the philosophy of tri dharma of higher education which are education, research, and contribution to the society. We have been always putting all of our efforts to implement this philosophy through our academic and social activities.

As we all know that the pace of development and advancement of technology, especially in electronics, is very fast. Therefore, Microelectronics Center ITB, being as a national research center in the topic of electronics, plays an important role to lead and to pioneering the development of electronics in Indonesia. Furthermore, as an effort to deepen the knowledge, to keep up to date with the latest development and advancement of technology, as well as to explore and to discover a new understanding in the field of science and technology, such a conference is held. I hope that by holding this conference and gathering all the academia from various countries, Microelectronics Center can always be the frontier in electronics technology and can give even bigger contribution to the development of Indonesia now and in the future.

Finally, we would like to express our sincere gratitude to the School of Electrical Engineering and Informatics (STEI) and Microelectronics Centers ITB and all the technical sponsors for their excellent supports in this conference.

We hope that the gathering of 2016 ISESD participants and experts from various countries can be as a media to exchange ideas and cultures can exchange many ideas and from each other and all of you will have a wonderful experience here in Bandung, Indonesia.

Welcome messages

Dr. Ir. Jaka Sembiring, M.Eng.

Dean of School of Electrical Engineering and Informatics

Institut Teknologi Bandung, Indonesia

Dear participants, guests ladies and gentlemen. Welcome to Indonesia, welcome to Bandung and welcome to the 2016 IEEE International Symposium on Electronics and Smart Devices (ISESD).

As the Dean of the School of Electrical Engineering and Informatics, Institut Teknologi Bandung (STEI ITB), it is my great honor to be able to welcome you to this conference.

This international conference is one of several international conferences organized by the School of Electrical Engineering and Informatics in 2016. These various conferences are related to our research groups in the school. The ISESD 2016 is closely related to the Electronics Engineering research group.

The topics discussed in this conference covers some very important subjects such as Devices, Circuits, and Systems, VLSI, Communication Systems, Multimedia and Systems, Signal Processing, Internet of Things, and Smart Devices. The research and development in these fields are of great importance for now and in the future.

I appreciate the participation of attendees coming from many countries such as Japan, Taiwan, Malaysia, Turkey, Vietnam, India, as well as participants from other countries including Indonesia.

In this occasion I would like to give my sincerely gratitude to my colleague, Muhammad Amin Sulthoni, as the General Chair of ISESD 2016 and his team for all their efforts in organizing this conference.

I hope that all of you will have a fruitful conference not only during presentation, discussion and technical sessions, but also during social and interpersonal communication from each other at the breaks, lunch, dinner and so on. I hope that the gathering of ISESD 2016 participants from various countries and cultures will bring a better understanding from each other and all of you will have enjoyable time here in Bandung, Indonesia.

Trio Adiono, ST., MT., Ph. D.

International Steering Committee Chair

Institut Teknologi Bandung, Indonesia

Welcome messages

On behalf of steering committee we would like to welcome all delegates travelling from various countries to the first 2016 IEEE International Symposium on Electronics and Smart Devices (ISESD) which is held in Bandung, known internationally as Paris van Java.

ISESD is held in order to accomodate all innovations and to anticipate the advancement of current state of the art of technology towards electronics and smart devices. As you may know that smart devices now become an integral part of our daily life. Many consumer apliances are now become a smart home appliances. In bigger ecosystems, we can also find the implementation of smart devices such as smart city, smart card, smart home, etc. Such smart devices are now become a trend that many companies as well as academia are pursuing towards it. Therefore, we hold this conference to facilitate many experts all around the world to discuss and to present their latest innovation in the area of smart devices technology.

Moreover, this conference is not limited to only certain areas, but we also open for multidiciplinary topics starting from devices, circuit & system, VLSI, communication systems, multimedia and systems, signal processing, and Internet of Things. It is because we believe that we can not get the best product of application without interacting with various areas of expertise.

We hope that in the future ISESD can cope with future challenges of smart devices technology, so that it can fullfill the society needs and even pushing a new technology that people may not think about yet. We also plan ISESD is not held in Bandung only, but spread out in other cities in Indonesia or even in the world.

Welcome messages

Dr. Eng. Muhammad Amin Sulthoni ST., MT

General Chair

Institut Teknologi Bandung, Indonesia

It is both a great pleasure and honor to welcome you all at the "2016 IEEE International Symposium on Electronics and Smart Devices (ISESD)", here in Mercure Bandung Setiabudi, Bandung, Indonesia.

ISESD is our first international conference which is organized by the National Center of Excellence of Broadband Wireless Access. This is a venue for exchange of information for researchers, academicians, and professionals through presentation of their new research ideas, innovations and development results as well as discussion of possible cooperation among the conference participants. We also hope the fruitful discussion in this conference can fullfil the gap among academia, researchers, professionals and industries that may enhance the benefit of technology for human life.

We are very pleased to have scholars and participants coming across several countries over the world with different interests and expertises. The conference is divided into 7 regular session topics with additional 2 special sessions. A series of the state of the art plenary sessions will be presented by 3 international renowned experts. It has been a real honor and privilege for us to serve as the General Chairs of the Conference. It is really our hope that you can find the conference inspiring, satisfying and enjoyable. We would like to thank to all keynote speakers, authors, and participants, and wish you have pleasant experience in Bandung, Indonesia.

On behalf of the organizing committee, we would like to thank to ISESD International Advisory/Steering Committee members, and all the organizing committee members for their valuable time and contribution to the excellent arrangement of this conference. This conference will not possible without the hard work of authors, reviewers, invited speakers, session chairs to make excellent technical program of this conference.

Finally, we would like to express our sincere gratitude to the School of Electrical Engineering and Informatics, Insitut Teknologi Bandung (ITB), Microelectronics Centers ITB, and all technical sponsors for their excellent supports.

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D5. Analog and Mixed Signals Processing

Design of Frequency Generator and Amplifier Level Converter Using 300nm CMOS Technology for Electro Capacitive Cancer Therapy (ECCT) Standard Operation Mode System

Febry Ramos Sinaga
Department of Electrical Engineering
University of Lampung
Bandar Lampung, Indonesia
febryramoss@gmail.com

Syaiful Alam
Department of Electrical Engineering
University of Lampung
Bandar Lampung, Indonesia
saifalam0@gmail.com

Muhamad Komarudin
Department of Electrical Engineering
University of Lampung
Bandar Lampung, Indonesia
m.komarudin@eng.unila.ac.id

Helmy Fitriawan
Department of Electrical Engineering
University of Lampung
Bandar Lampung, Indonesia
helmy.fitriawan@eng.unila.ac.id

***Abstract*—Electro capacitive cancer therapy (ECCT) system are constructed by six sub-systems, in this paper presented design and simulation for two sub-system in ECCT namely frequency generator and amplifier level converter. Design of two sub-system become first study for ECCT system can be applying to the IC technology. Design process begins with understand ECCT standard operation mode signal specification like input signal voltage, output signal voltage, form and frequency. Then using ring oscillator, negative clamper biased, two stage operational amplifier (op amp) circuits that estimated can produce those signal specification and layout them based on BSIM 3.1 MOSFET model using 300nm CMOS technology. Simulation result show that the system layout can produce 19Vpp, 100 kHz and asymmetric output signal from 5 volt DC input signal.**

Keywords—Electro Capacitive Cancer Therapy (ECCT); CMOS Technology; Ring Oscillator; Negative Clamper Biased; Operational Amplifier

I. INTRODUCTION

THE rapid growth of cancer disease in many countries has become an urgent crisis. The World Health Organization (WHO) research find 14.1 million new cases per year in 2012 and they will probably increase to 22 million cases per year in 2032. The most common cancers in 2012 are lung (1.8 million cases), breast (1.7 million cases), and large bowel (1.4 million cases) [1].

There are several conventional technologies that have been used for cancer medical treatment, such as radiotherapy, cryogenic and chemotherapy. However, these technologies are inflexible and operationally high-priced. Electro capacitive cancer therapy (ECCT) has become an alternative technology for cancer treatment. ECCT was invented by Dr. Warsito P. Taruno and friends at Ctech Labs EdWar Technnology based on Yoram Palti research about tumor treatment fields (TTF) [2]. ECCT work harness electric field low intensity and has good percentage to treat stadium IV cancer on soft tissues.

To reach optimum percentage, the ECCT must be used continuously in long-term with precise electric voltage and frequency. That continuously long-term application must be accompanied with durable electric power source and it should make the patient comfort. Durable electric power source can be obtained from minimize power dissipation while patient coziness can be obtained from minimize system dimension. By applying ECCT to 300nm CMOS technology, it will not only make the system power dissipation and dimension smaller but also the production cost will be cheaper [3].

In this work, the process of design, checking and simulation mask layout using ElectricVLSI and LTspiceIV software are described.

II. ECCT STANDARD OPERATION MODE

Electro capacitive cancer therapy (ECCT) system are constructed by six sub-systems, such as charger adapter, power supply, DC-DC converter, frequency generator, amplifier level converter (ALC) and electrode in apparel as in figure 1.

ECCT standard operation mode produces 20 volt peak-to-peak (Vpp), 100 kHz, and square shape signal output [2]. On

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ECCT standard operation mode, frequency generator function for converts 5 volt DC signal from DC-DC converter sub-system to 100kHz oscillation signal that has square shape, while amplifier level converter (ALC) will shift voltage level frequency generator output and amplify it to 20Vpp.

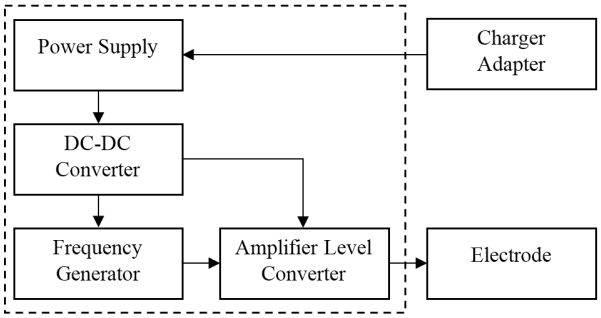

Fig. 1. ECCT System Block Diagram

A. Frequency Generator

Frequency generator sub-system is composed of ring oscillator circuit which is equipped with control voltage as shown in figure 2 [4].

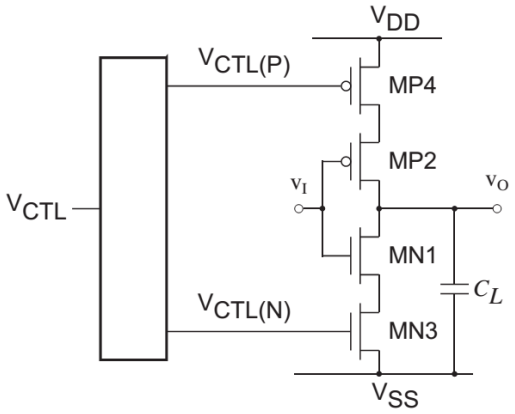

Fig. 2. Ring Oscillator Schematic

The ring oscillator and control voltage approach in this work adopt US patent 7,230,499 and each stage following unity voltage gain (gm) equation [5].

$$gm = \left(I_D \times K_P \times \frac{W}{L}\right)_{PMOS} + \left(I_D \times K_N \times \frac{W}{L}\right)_{NMOS} \quad (1)$$

Where:

$$K_P = \frac{\mu_P \cdot (\varepsilon_0 \cdot \varepsilon_{SiO_2})}{t_{ox}} \quad (2)$$

$$K_N = \frac{\mu_n \cdot (\varepsilon_0 \cdot \varepsilon_{SiO_2})}{t_{ox}} \quad (3)$$

So, as for determine the oscillation signal period and signal frequency that are produced by frequency generator, the following below equation is used:

$$T_{RF} = 2 \times \frac{1}{gm} \times C_{delay} \quad (4)$$

$$f_{osc} = \frac{1}{n \cdot T_{RF}} \quad (5)$$

Where T_{RF} is signal period on each stage, C_{delay} is capacitance load (C_L) [5] and n is number of ring oscillator stages [6].

B. Amplifier Level Converter

This sub-system is composed of negative clamper biased circuit and operational amplifier (op amp) circuit. The negative clamper biased serves to shift the voltage level, while op amp will amplify that shifted signal to 20Vpp. The op amp circuit which is used in this work adopt two stage op amp methodology [3][7] as shown in figure 3.

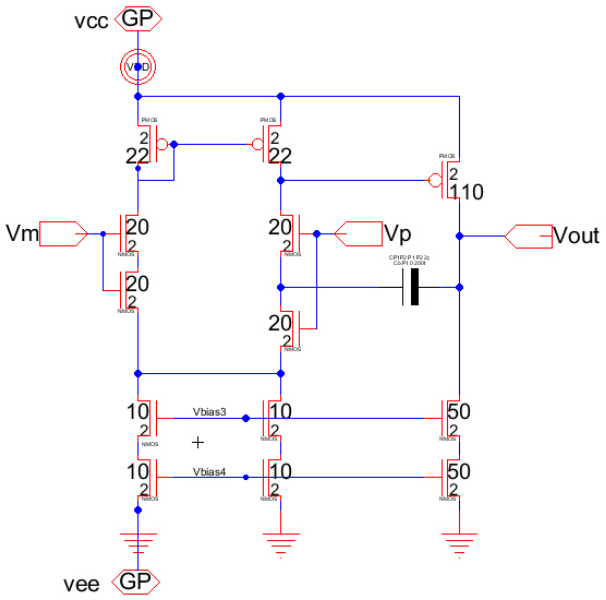

Fig. 3. Amplifier Level Converter Schematic

III. Mask Layout System Design

The data which is used in this layout design process comes from ECCT standard operation mode signal specification, BSIM3 models for AMI semiconductor C5 process, MOSIS scalable CMOS (SCMOS) design rules and default parasitic project value in ElectricVLSI.

A. Frequency Generator Layout

For generating 100 kHz and forming square shape output signal from 5 volt DC input signal, frequency generator layout composed of 7 stages ring oscillator and drives strength control is voltage. The total number of transistor used in this sub-system are 16 NMOS and 15 PMOS component which are interconnected in series and parallel as shown in figure 4.

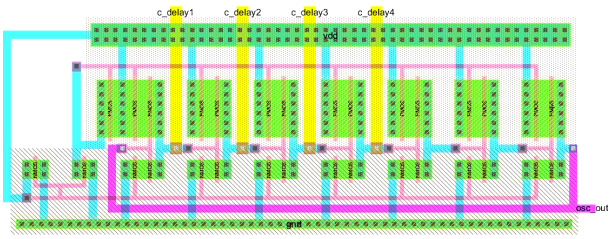

Fig. 4. Frequency Generator Mask Layout for ECCT Standard Operation Mode

The W/L ratio using in layout of PMOS is 30/2 and NMOS is 10/2. That ratio used for make signal rise time same as signal fall time, so the output signal can begin oscillate from 2,5 volt and forming square shape. In addition to NMOS and PMOS components, frequency generator also requires 300pF capacitor on stage 1 to stage 4 for increase the delay time frequency generator. Due to very large layout are needed 300pF capacitor is just simulated with value on every c_delay pin.

B. Amplifier Level Converter

Negative clamper biased layout is composed of a 500kΩ resistor, two capacitor and 1N4148 diode model from diode.inc as shown in figure 5.

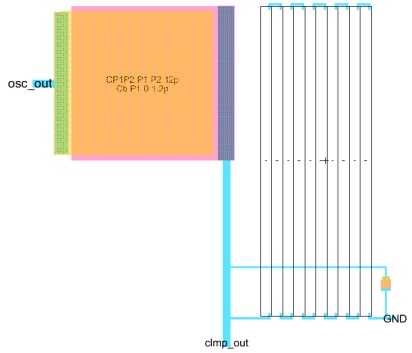

Fig. 5. Negative Clamper Biased Mask Layout

Operational Amplifier layout is composed of 13 NMOS, 25 PMOS and a compensation capacitor as shown in figure 6.

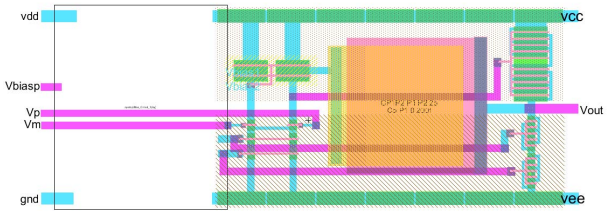

Fig. 6. Operational Amplifier Layout

All components and sub-systems above have been checked following DRC, ERC and LVS tools in ElectricVLSI. Beside that the total layout areas that needed to layout all frequency generator and amplifier level converter sub-system is 0.52mm×0.52mm or 0.2704mm^2.

IV. Simulation Result And Discussion

In this work, each sub-system layout is simulated by including the parasitic effect using ElectricVLSI and output signal viewed in graphical form using LTspiceIV software.

Figure 7 shows the output signal from frequency generator layout. From figure 6 it can be seen that frequency generator can produce 100.01 kHz and square shape signal. The parasitic effect does not affect the frequency generator performance.

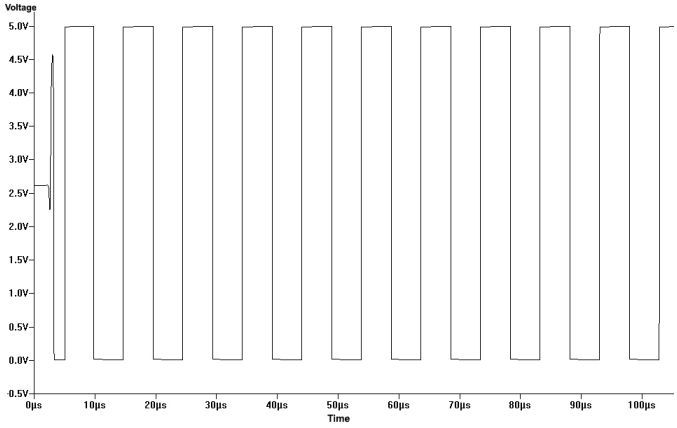

Fig. 7. Output Signal of Generator Frequency Layout

Figure 8 shows the output signal from negative clamper biased layout after receiving 100.01 kHz and square shape signal from frequency generator.

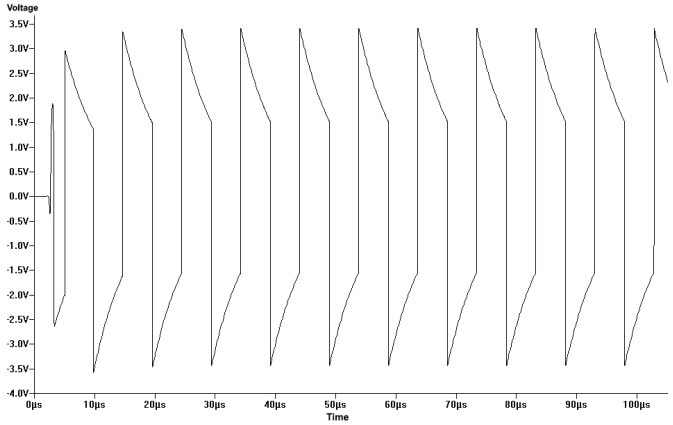

Fig. 8. Output Signal of Negative Clamper Biased Layout

It can be seen the signal voltage level shift 2.5 volt toward negative x-axis and keep oscillating on frequency 100.01 kHz, but the shape of signal is not square anymore. That is due to capacitor and resistor value not big enough. Bigger value of capacitor or resistor will increase the "charging" and "uncharging" circuit time constant which affecting the stability of the output signal. Moreover, bigger resistor and capacitor value need bigger layout area which result in the amount of system layout area and production cost.

Figure 9 shows the output signal from op amp layout after receiving negative clamper biased`s signal. This figure also shows the result of full layout system output.

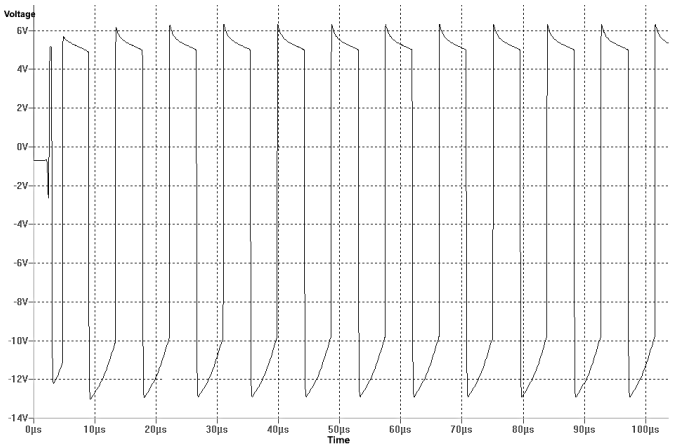

Fig. 9. Output Signal of Op Amp

As be seen, the output signal oscillate on frequency 100kHz and has 19Vpp voltage range, but there are several phenomena that affect to the output signal. That phenomenon are shifting of the signal to the negative x-axis direction and asymmetric signal form. Shifting of the signal does not make the output signal begin to oscillate from 0 volt but from -0.47 volt and becomes one of the asymmetric signal forming factors. That phenomena can be occurs because op amp layout have an offset voltage characteristic. Moreover the asymmetric signal form occurs because common-mode rejection ratio (CMRR) op amp characteristic. Effect of parasitic affect to the asymmetric differential amplifier stage performance in op amp so that the CMRR value become less and produce the asymmetric output signal. For better layout system performance, improvement can be done with change the clamper circuit and increase the CMRR value along decrease the offset voltage with change or modify the op amp methodology circuit.

V. CONCLUSIONS

In this work, mask layout design of frequency generator and amplifier level converter using 300nm CMOS technology has been made. This layout design intended for two sub-system from electro capacitive cancer therapy (ECCT) standard operation mode system. From the simulation results is known that the layout design can produce signal frequency and voltage output corresponding to the ECCT standard operation mode system that Ctech Labs EdWar Technology manufactured but cannot meet the characteristic of signal shape and voltage level from that system. Future research will be directed to improvement of the amplifier level converter layout system performance and make the layout of DC-DC converter sub-system so that every ECCT sub-system can be packaging in an IC with CMOS battery as a power supply.

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